# MIL-STD-1553 Remote Terminal Software Migration Guide

# DDC® Enhanced Mini-ACE® RT to Holt RT

## Devices Supported
## HI-6120, HI-6121
## HI-6130, HI-6131
## HI-6135, HI-6136
## HI-6137, HI-6138

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# 1 INTRODUCTION

This application note can be used as a guide for migrating RT software developed for any of the DDC Enhanced Mini-ACE compatible Remote Terminal Devices to any of the Holt Remote Terminal Devices. This is done through the development of a specific example configuration implemented for both devices. Important differences and similarities in configuration or operation are highlighted.

Initially, the example RT configuration will illustrate the programming steps necessary to initialize each device's registers and memory and enable the terminals into an online state. Then detailed reviews will show the memory maps and data structure differences. Finally the user data buffer types and method for servicing the device either through interrupts or polling are demonstrated.

# 2 EXAMPLE CONFIGURATION

For the example, four subaddresses plus mode codes will be configured with various user data buffer options and interrupt conditions. The example will illustrate the steps necessary to initialize the registers and enable the terminal into an on-line operational state.

**Subaddress 1:** Transmit, Single Message Buffer, Enable Interrupts when a message is transmitted.

**Subaddress 7:** Receive and Broadcast Receive, 1024-word circular buffer, Enable interrupts when the circular buffer rolls over.

**Subaddress 19:** Receive and Broadcast, Ping Pong (Double) Buffer, Enable interrupts every time a message or broadcast message is received.

**Subaddress 30:** Receive, Transmit, and Broadcast: Configured as the wraparound subaddress, Single Message Buffer, No Interrupts Enabled

Table 1 - Illustrates the steps required to initialize the Holt HI-6130 RT as compared to the steps required to initialize the DDC Enhanced Mini-ACE RT. The initialization sequence is quite similar between the two devices.

**Table 1 - Initialization Steps**

| Tasks: | Holt HI-6130 | DDC EMACE |
|---|---|---|
| **Reset** | HW Master Reset | Perform SW Reset by writing 0x0001 to Start/Reset Register |
| **Initialize Register Settings** | Initialize Master Configuration Register | Initalize Config Register #2 for Enahnced RT memory management or Separate Broadcast options. Set Time Tag Resolution. Enhanced Interrupts enabled? Level/Pulse* interrupts. Clear Service Request Bit ? |
| | Initialize RT1 Configuration Register | Initialize Config Register #3 |
| | Initialize the Hardware and RT1/RT2 Interrupt enable and Interrupt output registers | Initalize Interrupt Mask Registers #1 and #2 |
| | RT1 Operational Status Register | Initialize Config Register #4 |
| | Time Tag Counter Configuration Register | Initialize Config Register #5 |
| | N/A | Initialize Config Register #6 |
| **Load Address of descriptor table or stack location.** | Load the address of the RT1 Descriptor Table into the RT1 Descriptor Base Address Register | Load the starting location of the Descriptor Stack into Active Stack Pointer location is |
| **Initialize descriptor blocks and look up tables** | N/A | Initialize the Descriptor Stack Memory to 0x0000 |
| | Initialize the descriptor table and load control words for all legal subaddress and mode commands. This includes interrupt options and data buffer pointers. | Initialize the Active Area Look up table. The lookup table address for each T/R/B SA should be initialized at a pointer value. For enhanced RT memory management also intialize the SA control words for memory management and interrupt options. |
| **Legalization** | Initialize the Illegalization Table if illegalization is to be used. | Initialize the Illegalization Table if illegalization is to be used. |
| **Busy Response** | N/A - Subaddress Busy response is configured in the descriptor table control word | If the BUSY LOOKUP Table is enabled, program the busy table. |
| **Mode Code Interrupts** | N/A - Simplified Mode Code Handling is enabled and Data Words, MIW, and TTW are stored in descriptor table. Mode code interrupts are configured in the descriptor table control word. | If ENHANCED INTERRUPTS AND ENHANCED MODE CODE HANDLING IS ENABLED, then Interrupts for selective mode codes are programed in locations 0x0108 through 0x010F. |
| **Initialize Data Blocks** | Initalize Transmit Blocks with Data to be Transmitted | Initialize transmit data blocks with data to be transmitted. |
| | | Initialize Rx datablocks with 0x0000 |
| **Enable RT Execution** | Enable the RT by setting the RT1STEX bit in the Master Configuration Register. | Enable the RT by writing to Config Register 1. Set bit 15 and clear bit 14. Select current Active Area by setting or clearing bit 13. |

## 2.1 Initialization Steps Compared

The DDC device has many settings spread across various registers. We will look at some of these settings in more detail and see how they are simplified within the Holt Register Map. For the example, certain assumptions were made about how the Enhanced Mini-ACE RT is configured for common implementations. Those assumptions are as follows:

1. Enhanced Mini-ACE ENHANCED MODE is enabled. There is no equivalent in the Holt Devices because it is not necessary. RT features supported by DDC's ENHANCED MODE have equivalent support by default in the Holt Remote Terminal.

2. Enhanced Mini-ACE ENHANCED INTERRUPTS are enabled. Holt vs. DDC interrupts are covered in detail in Section 6 INTERRUPTS AND POLLING OPTIONS
3. Interrupts for RT Subaddress CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT MODE CODE, and FORMAT ERROR are enabled.
4. BROADCAST SEPARATION is implemented. (for MIL-STD-1553B Notice 2 compliance)
5. Enhanced Mini-ACE ENHANCED MEMORY MANAGEMENT and OVERWRITE INVALID DATA are enabled, and 256-WORD BOUNDARY DISABLED is disabled. There is no equivalent setting in Holt Remote Terminals. The Holt RT already supports advanced memory management features by default, providing equivalent functionality.
6. Time Tag Resolution of 64 µs/LSB (default) is selected.
7. Busy by subaddress is enabled. However, all subaddresses are initially programmed as "not busy."
8. A loopback test failure will cause the RTFLAG bit to become set. Holt device does not have an RTFLAG bit but provides equivalent functionality in that the LBFA and LBFB bits become set and an interrupt can be optionally generated.
9. Enhanced Mini-ACE ENHANCED MODE CODE HANDLING is enabled. The Holt Remote Terminal provides a similar functionality called Simplified Mode Code Processing which is described in more detail in Section 8 MODE COMMAND PROCESSING
10. An RT address of seven (7) is assigned.
11. All used subaddresses, as well as all MIL-STD-1553B mode codes except selected transmitter shutdown and override, are programmed as legal. This includes the associated broadcast commands, where appropriate. All unused subaddresses and mode codes, and undefined and reserved mode codes are illegalized.
12. The (single) Data Word Buffer for TX SA1 is initially loaded with transmit data of 0x0000, 0x0001, through 0x001F.

# 3 MEMORY MAP

Table 2 shows a typical HI-613x Memory Map when using only a single Remote Terminal. This memory map will be similar for all Holt devices. Notice that the Holt device supports two fully independent Remote Terminals. For the purposes of this example only Remote Terminal 1 will be configured, however the steps would be the same to configure Remote Terminal 2. The Holt memory map can be compared to DDC Enhanced Mini-ACE RT memory map shown in Table 3.

**Table 2 - Holt HI-613x RT Memory Map**

| Address | Description | Comments |
|---|---|---|
| 0x0000-0x004F | Registers | Lower 80 memory locations are reserved for Registers |
| 0x0050-0x0053 | Reserved | Not used in RT Example |
| 0x0054-0x01DF | Not used in RT Example | Not used in RT Example |
| 0x0180-x01BF | 64 Word Interrupt Log Data Buffer | Chronological History of Interrupt Events |
| 0x01C0-0x01DF | RT 1 Temporary Rx Buffer | Not normally used by Host |
| 0x01E0-0x01FF | RT2 Temporary Rx Buffer | Not used in this RT Example |
| 0x0200-0x02FF | RT1 Command Illegalization Table | Same as DDC but offset for RT1 is at 0x0200 vs. DDC at 0x0300 |
| 0x0300-0x03FF | RT2 Command Illegalization Table | DDC does not support multiple independent RTs. |
| 0x0400-0x04FF | RT 1 Descriptor Table Default | Similar to DDC Enhanced Mini-ACE RT lookup table however multiple lookup tables can be used, whereas DDC only supports area A and B. Active area is configured by Descriptor Table Base Address Register. |
| 0x0500 - 0x05FF | RT 1 Mode Code Descriptor Table | Includes mode command descriptor blocks, interrupt configuration and if simplified mode command processing is enabled will inlcude Data Word, Message Information Word, and Time Tag Word. |
| 0x0600-0x06FF | RT 2 Descriptor Table Default | DDC does not support multiple independent RTs |
| 0x0700 - 0x07FF | RT 2 Mode Code Descriptor Table | DDC does not support multiple independent RTs |
| 0x0800-0x7FFF | Host Allocated RAM used for Data Buffers etc. | Used for datablocks etc. |

One difference between the Holt and DDC RT is the simplified memory map of the Holt RT. For example, the main configuration is done through a single descriptor lookup table with the Holt RT, whereas, with DDC there are several lookup tables required to accomplish the same configuration. This is described in more detail in Section 4 HOLT DESCRIPTOR TABLE VS. DDC LOOKUP TABLES

**Table 3 - DDC Enhanced Mini-ACE Typical RT Memory Map**

| Address | Description |
|---|---|
| 0x0000-0x00FF | Stack A |
| 0x0100 | Stack Pointer A |
| 0x0101 | Global Circular Buffer A Pointer |
| 0x0102-0x0103 | RESERVED |
| 0x0104 | Stack Pointer B |
| 0x0105 | Global Circular Buffer B Pointer |
| 0x0106-0x0107 | RESERVED |
| 0x0108-0x010F | Mode Code Selective Interrupt Table |
| 0x0110-0x013F | Mode Code Data |
| 0x0140-0x019F | Lookup Table A |
| 0x01A0-0x01BF | Subaddress Control Word Lookup Table A |
| 0x01C0-0x021F | Lookup Table B |
| 0x0220-0x023F | Subaddress Control Word Lookup Table B |
| 0x0240-0x0247 | Busy Bit Lookup Table |
| 0x0248-0x025F | (not used) |
| 0x0260-0x027F | Data Block 0 |
| 0x0280-0x02FF | Data Block 1-4 |
| 0x0300-0x03FF | Command Illegalizing Table |
| 0x0400-0x041F | Data Block 5 |
| 0x0420-0x043F | Data Block 6 |
| • | • |
| • | • |
| 0x0FE0-0x0FFF | Data Block 100 |

# 4 HOLT DESCRIPTOR TABLE VS. DDC LOOKUP TABLES

One of the main differences between the Holt RT and DDC RT are how the subaddresses are configured. The Holt RT uses the Descriptor Table to enable message interrupts, specify RAM data buffer locations, and manage individual subaddress Busy Bit behavior. Each RT uses a Descriptor Table consisting of 128 consecutive "descriptor blocks". Each descriptor block is comprised of four 16-bit words. There are four quadrants of 32 four-word blocks. The default starting location for the RT1 Descriptor Table is 0x0400 which was set by writing to the Descriptor Table Base Address Register. The structure of the Holt Descriptor Table is shown in Figure 1.

The First word in each descriptor block is the Control Word. For Subaddress Tx/Rx commands, the Control Word is used to configure the interrupt behavior, busy bit behavior, and the type of data buffer associated with the subaddress. The control word also has bits that can be polled to see if that subaddress was accessed or a broadcast command was received.

Subsequent Descriptor words in the descriptor block contain pointers to the data blocks for subaddress commands. For Mode Codes, with Simple Mode Code Processing enabled, the mode code data words, Message Information Word, and Time Tag Word are also contained within the descriptor block.

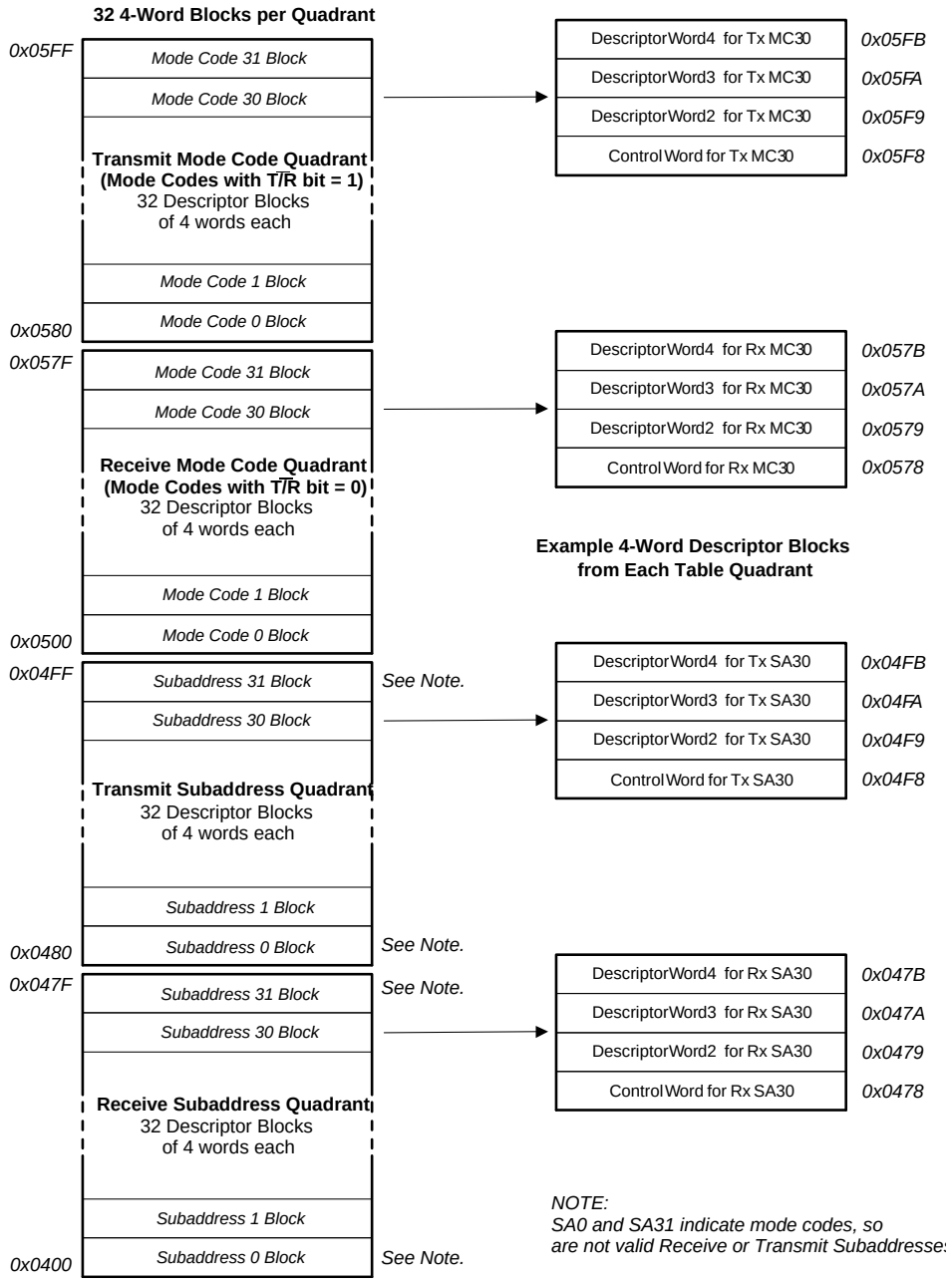


**Figure 1 - Holt RT Descriptor Table**

The DDC Enhanced Mini-ACE RT uses a lookup table which contains pointers to the data buffer and optionally supports a subaddress control word lookup table that controls interrupt behavior and data buffer management schemes for each subaddress.

There are several important differences between the Holt Descriptor Table and the DDC lookup tables enumerated below:

1. The Holt Descriptor Table can be used to configure busy bit response whereas with DDC there is a separate busy bit lookup table to control that behavior.
2. The Subaddress Control Words and Data Buffer Pointers are within the same descriptor block, whereas DDC uses separate lookup tables.
3. In the Holt RT, Mode Code Data can optionally be stored within the descriptor block rather than a separate user buffer, simplifying Mode Code processing. With DDC Enhanced Mode Code processing, the Mode Code Data Words are stored in a fixed memory location.
4. With Holt, Mode Code Interrupts are configured within the control word, whereas with DDC they are configured in a separate fixed memory location.
5. With the Holt RT multiple descriptor tables can be configured. The specific table used can be enabled simply by updating the RT Descriptor Table Address Register. The DDC RT is limited to an Active area A and Inactive Area B. This gives the Holt RT greater flexibility for quickly changing the configuration.

# 5 USER DATA BUFFERS

In general the Holt Remote Terminal supports equivalent data buffering and memory management schemes to those available in the DDC Enhanced Mini-ACE RT. Familiar buffer management options makes for easy porting of software from DDC to Holt.

## 5.1 Holt Index/Single Buffer Mode vs. DDC Single Buffer Mode

The most basic data buffer type in the DDC Enhanced Mini-ACE RT is single buffer mode. This mode is fully supported by Holt. With single buffer mode, new messages are written to or read from a single data buffer. However, the Holt Index Buffer does offer the user some additional functionality that can be optionally used.

For the purposes of this example, we are using the Index Buffer with INDX = 0, which provides the equivalent functionality to the DDC Single Buffer Mode. For more information about using non-zero INDX values, please reference the HI-613x Datasheet.

For Index Single Buffer mode the descriptor block is as follows:

| | |
|---|---|
| Descriptor Word 1 | Control Word |
| Descriptor Word 2 | Data Pointer A |
| Descriptor Word 3 | INDX Index Word |
| Descriptor Word 4 | Broadcast Data Pointer |

As the name implies, Message Information and Data are stored in a single 34 Word Buffer. Consisting of a Message Information Word (MIW), and Time Tag Word (TTW) and up to 32 data words. A separate data block can be allocated for Broadcast data in accordance with the requirements of MIL-STD-1553B.

This mode differs slightly from the DDC configuration where the data and message information are stored separately. With the DDC RT, the user must first find the message information on the RT Descriptor Stack and then get the data words from the data buffer/block.

The Index Single Buffer Mode is shown in Figure 2 below:

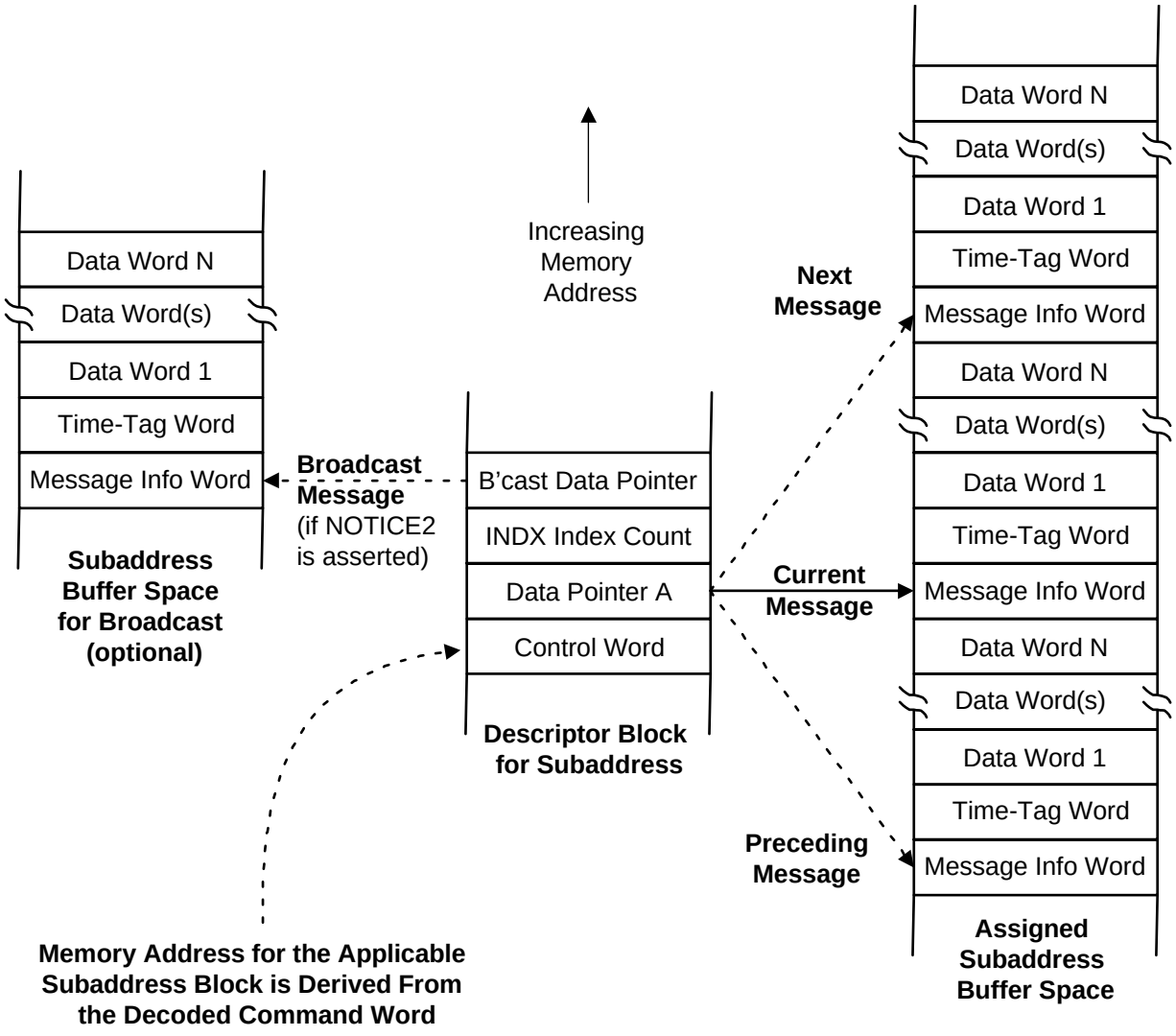


**Figure 2 - Illustration of Index Buffer Mode**

Upon successful message completion, if non-zero the INDX count in Descriptor Word 3 is decremented. If decremented result is non-zero, Data Pointer A is adjusted so next message is

stored above just-completed message. If decremented INDX is zero, Data Pointer A remains static and IXEQZ interrupt occurs if enabled in Control Word. INDX = 0 provides equivalent functionality to the DDC single buffer mode. The user can choose to use non-zero INDX for additional flexibility.

## 5.2 Ping-pong (Double) Buffer Mode

Ping-pong (Double) buffer mode is a method for storing message and time-tag information and data associated with messages. Each unique MIL-STD-1553 subaddress or mode code can be assigned a pair of data buffers for transmit commands and a pair of data buffers for receive commands. The device retrieves buffer data for transmit commands, or stores buffer data for receive commands. During ping-pong operation, the device alternates message storage between Data Buffer A and Data Buffer B, on a message-by-message basis.

In general, Ping-pong (Double) buffering is used to guarantee data consistency for receive subaddresses. In fact, the DDC terminal only supports double buffering on receive subaddresses. It is generally not desirable to use double buffering for transmit subaddresses, where host software can better manage data consistency. When a subaddress or mode command uses ping-pong data buffer mode, its 4-word descriptor block in the Descriptor Table is defined as follows:

| | |
|---|---|
| Descriptor Word 1 | Control Word |
| Descriptor Word 2 | Data Pointer A |
| Descriptor Word 3 | Data Pointer B |
| Descriptor Word 4 | Broadcast Data Pointer |

In the case of the Holt RT, again both message information and data are stored in the same buffer. Whereas with DDC, the message information is held in the RT descriptor stack and only the data is kept in the buffer.

Message processing alternates between Data Buffers A and B. Upon successful message completion, the DPB bit in Descriptor Control Word is updated so next message uses other buffer. Buffers are overwritten every other message. A separate buffer for broadcast messages is optional. There is no alternate buffer for successive broadcast messages.

Because ping-pong messages and host processor servicing are asynchronous, there is potential for “data collision”. For example, the host reads data from an earlier message while the device simultaneously writes new message data to the same buffer. The host reads a mix of new and old message data. Collisions can occur for both transmit and receive messages. A handshake scheme lets the external host asynchronously service ping-pong data buffers without data collision. This is described in more detail in the HI-613x Datasheet. Holt Ping-pong buffer mode is illustrated in Figure 3.

Holt offers configuration options which prevent toggling of the data buffer A/B pointer (DPB) when the message ends in RT Busy status, or when the command is illegal. Consider the case where a particular subaddress has a combination of legal and illegal word counts; illegal counts do not toggle the DPB pointer. These configuration options assure data integrity because the DPB buffer pointer only toggles upon completion of messages which successfully transact data.

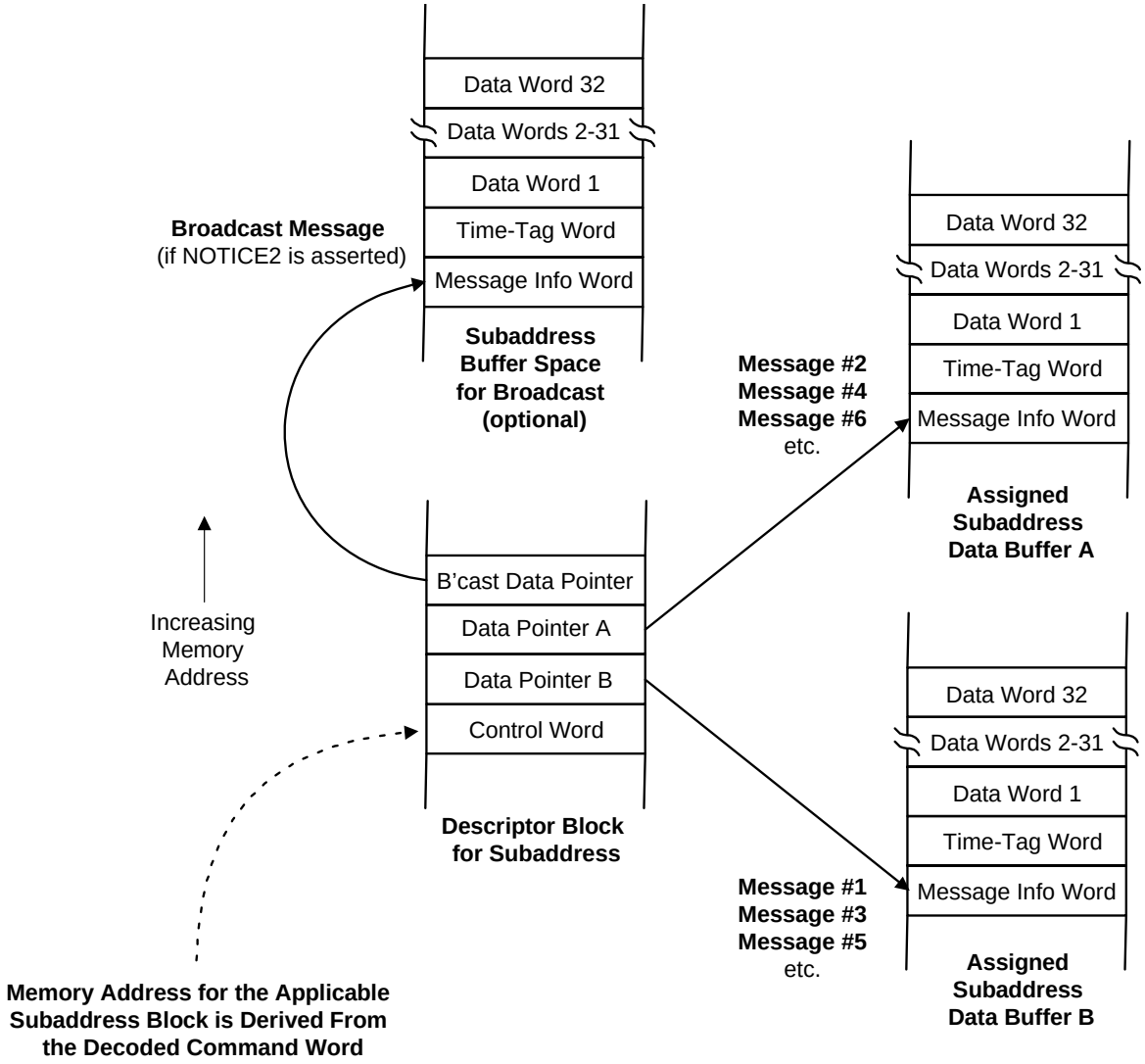


**Figure 3 - Illustration of Holt Ping-Pong (Double) Buffer Mode**

## 5.3 Circular Buffer Modes

Both Holt and the DDC terminals implement RT circular buffer modes, but the implementations do have some differences worth noting. The DDC RT supports an option for a global circular buffer which the Holt RT does not support.

For the standard subaddress circular buffers, Holt supports two types; data block completion for one is predicated by a fixed number of messages while the other is predicated by 100% buffer fulfillment. Holt Circular Buffer Mode 2 is the closest to the DDC implementation because in both cases the data and message information are stored separately. Conversely, Holt does offer Circular Buffer Mode 1 in which data and message information are stored in the same buffer. Circular Buffer Mode 1 is an option not supported by DDC.

For the purpose of this example, Circular Buffer Mode 2 (block completion by number of messages) was used since it is closest to the DDC implementation. Segregated storage for data and message information simplifies host loading / offloading of buffered data. The descriptor MIB Address tracks number of messages. Full count occurs when N initialized 0-bits become N 1-bits. When full number of messages in block is transacted, an optional interrupt is generated to notify host. For Circular Buffer Mode 2, the Descriptor block is defined as follows:

| | |
|---|---|
| Descriptor Word 1 | Control Word |
| Descriptor Word 2 | SA (Buffer Start Address) |
| Descriptor Word 3 | CA (Buffer Current Address) |
| Descriptor Word 4 | MIBA (Message Info Buffer Addr) |

The illustration for Circular Buffer Mode 2 is shown in Figure 4.

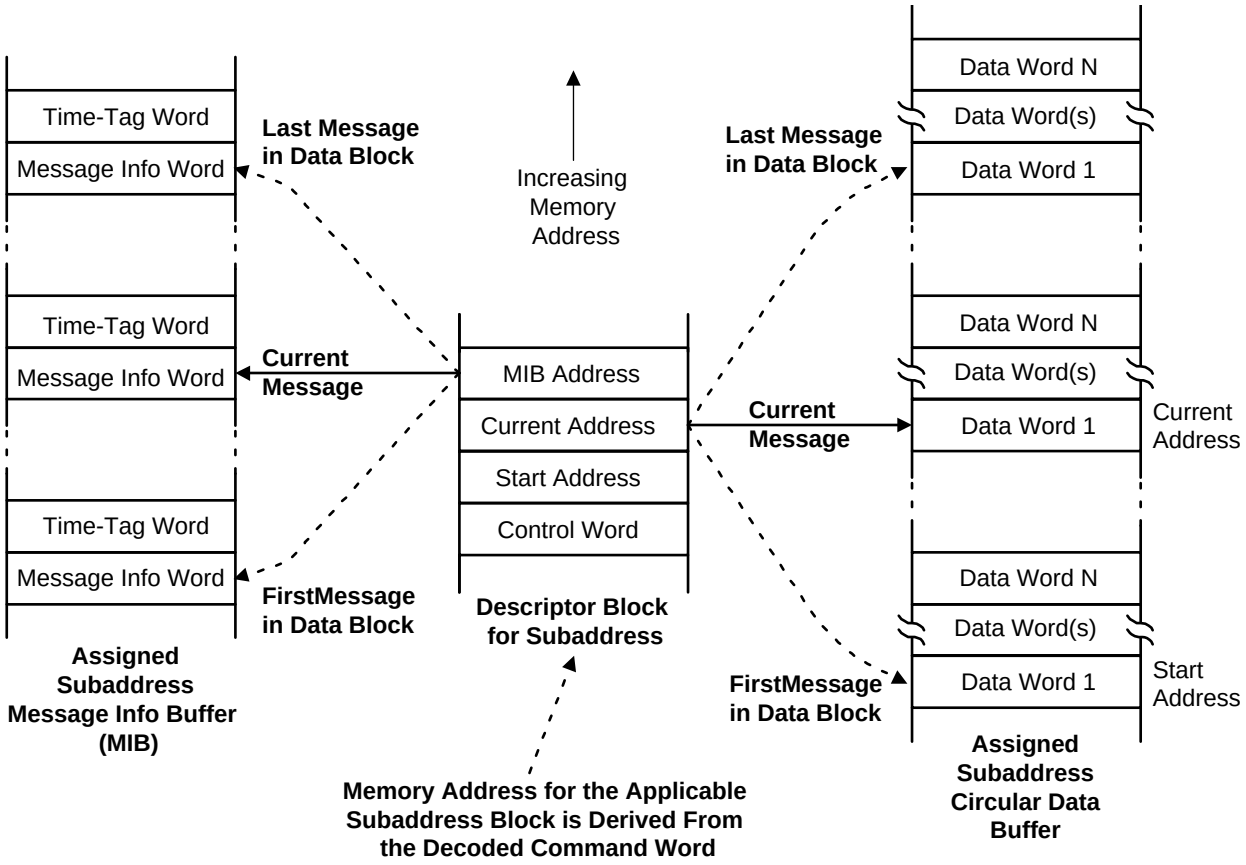


**Figure 4 - Circular Buffer Mode 2 Illustration**

# 6 INTERRUPTS AND POLLING OPTIONS

Software written for the DDC Enhanced Mini-ACE RT may use several methods for determining when a message has been processed. These methods support both polling and/or interrupt driven software. For Interrupts, a comparison is shown in Table 4 for the supported interrupt conditions. Notice that Holt does not support an RT Descriptor Stack (Command Stack) this is discussed in more detail in Section 7 SERVICING RT SUBADDRESS MESSAGES.

**Table 4 - Comparison of Holt and DDC Interrupt Conditions**

| DDC | Holt | Comments |
|---|---|---|
| End-of-(every)Message | Interrupt When Accessed (IWA) | Holt can setup end of message interrupts in subaddress or mode code control word |
| Message Error | Message Error | Same |
| Selected (transmit or receive) Subaddress | Interrupt When Accessed (IWA) | Same |
| 100% Circular Buffer Rollover | Index Equals Zero (IXEQZ) | Same |
| 50% Circular Buffer Rollover | Not Supported | Not Supoprted |
| 100% Descriptor Stack Rollover | N/A | Holt device does not have an RT command stack |
| 50% Descriptor Stack Rollover | Not Supported | Holt device does not have an RT command stack |
| Selected Mode Code | Interrupt When Accessed (IWA) | Holt can setup end of message interrupts in subaddress or mode code control word |
| Transmitter Timeout | Transmitter Timeout (WDTX) | Same |
| Illegal Command | Illegal Command | Same |
| Interrupt Status Queue Rollover | Interrupt Log Buffer | Holt provides several ways to determine current level of interrupt log buffer by IRQ or polling. |
| Not Supported | Broadcast Command Received (IWB) | Holt can setup end of message interrupts in subaddress or mode code control word |
| Not Supported | RAM Error Detected/Corrected (RAMERR) | DDC does not support EDAC |
| RAM Parity Error is supported | RAM Error Detected/Not Corrected (UNCRE) | DDC does not support EDAC. RAM Parity error is supported on MAMBA devices. |
| Format Error | Loopback Fail Interrupt (LBFA/LBFB) | With DDC Host must get additional information about the FORMAT ERROR from the BSW. |
| Not Supported | Time Tag Match (TTM) | Holt can set an interrupt when Time Tag matches a certain value. |
| RT ADDRESS PARITY ERROR | Terminal Address Parity Fail (RTAPF) | Same |
| Not Supported | Remote Terminal Interrupt Pending (RTIP) | Host can poll or get IRQ from any supported RT interrupt. |

In addition to the interrupt conditions described above, there are several polling methods that may be used.

Table 5 provides a brief comparison of these options.

**Table 5 - Comparison of Holt and DDC Polling Options**

| DDC | Holt | Comment |
|---|---|---|
| Stack Pointer RAM Location | Interrupt Count and Log Address Register | Holt does not have a stack but current location and Interrupt count can be polled. |
| RT Last Command Register | RT Current Command Register | Same |
| Interrupt Status Register Bits | Interrupt Pending Registers | Holt has greater flexibility in quickly decoding pending interrupts. Described in greater detail in the following sections. |
| Control Word EOM | Interrupt When Accessed (IWA) | Same |
| Particular Mode Code - Selective Interrupt Table | Interrupt When Accessed (IWA) | Holt does not need a separate lookup table. |
| RT Subaddress Control Word Register | RT Current Control Word Adress Register | Same |
| Not Supported | RT Current Message Information Word Register | Provides access to current MIW |
| Not Supported | Subaddress Control Word DBAC Bit | Host can poll DBAC bit in specific control words for activity. |

The HI-613x Remote Terminal Interrupts are controlled by two register triplets. One 3-register set is for hardware and the other is for the Remote Terminal itself. Using these registers, it is possible for the user to setup multiple levels of interrupt priority, whereby high priority interrupts will generate a hardware IRQ and lower priority interrupts will not generate the IRQ, but will still set bits in the appropriate pending interrupt register which may be polled. In addition the Hardware Interrupt Pending Register provides a means for quickly decoding where an interrupt originated by looking at only three bits.

Holt Remote Terminals also support the use of the Interrupt Log Buffer, which provides 32 entries each consisting of two 16-bit words that give the user information about the interrupt as well as a chronological history of interrupts events. A description of the interrupt log buffer entries is shown below in Figure 5. Holt HI-613x interrupt behavior and polling options are described in much greater detail in the respective datasheets.

| Interrupt Type | Interrupt Identification Word (IIW) | Interrupt Address Word (IAW) |
|---|---|---|
| Hardware | Matches format of Hardware Pending Interrupt Register 0x0006 | Always 0x0000 |
| Remote Terminal RT | Matches format of Remote Terminal Pending Interrupt Register (0x0009), **EXCEPT** if INTBUSY bit 2 is set in Extended Configuration Register (0x004D), then bit 9 of RT Interrupt Information Word serves as WASBUSY status flag, asserted if terminal was BUSY when message interrupt occurred. See Section “Extended Configuration Register (0x004D)”. **Note:** Busy status is not an interrupt causing event. | RT Descriptor Table address pointing to the Command Word of the message in which interrupt occurred |

**Figure 5 - Interrupt Log Buffer Entry Description**

# 7 SERVICING RT SUBADDRESS MESSAGES

Another difference between the DDC Enhanced Mini-ACE RT and the Holt HI-613x RT is DDC's use of the RT descriptor stack (command stack). For the DDC terminal the stack is where message information is kept along with a pointer to the message data buffers. In the DDC implementation the stack contains a chronological history of message information or descriptor blocks. Each descriptor block contains a Block Status Word (BSW), a Time Tag Word (TTW), a pointer to the data block, and the received command word. To service the DDC RT messages the host must go through the stack looking for messages and then get the message data from the data block.

With the Holt Remote Terminal there are a variety of flexible ways to service RT messages. The descriptor table will contain the pointer to the data buffer containing the Message Information Word (MIW) and the Time Tag Word (TTW) for Index (Single) Buffer, double buffer, and Circular Buffer Mode 1. As mentioned previously, circular buffer mode 2 provides a separate MIB buffer with the MIW and TTW. If the user needs the chronological history of messages or events, then the Interrupt Log Buffer can be utilized. For each RT message entry in the log buffer, the Interrupt Address Word will contain a pointer to the descriptor table entry for which the interrupt condition occurred. Alternatively, the DBAC bit of specific subaddress control words can be polled for activity as mentioned previously.

# 8 MODE COMMAND PROCESSING

For the purposes of this example, the assumption was that for the DDC RT ENHANCED MODE CODE HANDLING was enabled. The Holt RT provides a similar functionality called Simplified Mode Code Processing. When the SMCP option bit in the RT Configuration Register is asserted, individual data words for mode codes 16-31 decimal are stored within the Descriptor Table. Simplified Mode Command Processing is a global option applying to all mode commands. When the SMCP bit is high, mode command descriptor blocks (in the Descriptor Table) do not contain data pointers to reserved buffers elsewhere in the shared RAM. Instead, each 4-word descriptor block itself contains the message information word, the time-tag word and the data (mode codes 16-31 only) from the most recent occurrence of each mode command as shown below:

| | |
|---|---|
| Descriptor Word 1 | Mode Command Control Word |
| Descriptor Word 2 | Message Information Word |
| Descriptor Word 3 | Time-Tag Word |
| Descriptor Word 4 | Mode Data Word |

For the three defined transmit mode commands with data, Descriptor Word 4 contains the last value transmitted by the RT when responding to that same mode code command. For two transmit mode commands, the data word transmitted does not originate from that location. For MC18 “transmit last command”, the data word is automatically provided by the device, based on the RT’s last valid command. For MC19 “transmit BIT word”, the data word originates from one of two registers selected by the ALTBITW option in the RT Configuration Register. For both MC18 and MC19, the transmitted data word is automatically recorded in the mode command’s Descriptor Table word 4 after message completion. For all other transmit mode commands 16-31 (decimal), the device reads the data word for transmit from Descriptor Table word 4, assuming SMCP is enabled. For all mode commands, the Message Information and Time-Tag words are also updated at message completion.

# 9 MESSAGE INFORMATION WORD (MIW)

For the Holt Terminals, message information is stored in the Message Information Word (MIW). For both subaddress commands and mode commands, the MIW can be thought of as an equivalent to the DDC Block Status Word (BSW). The MIW contains information about message error conditions, if the message was and RT-RT transfer, which bus the message occurred on, if the command was legal, if the terminal responded with BUSY bit set, and the word count of the message. Additional information about the message is available in the subaddress control word, for example was the message a broadcast message.

Note that the command word itself is not directly available in the Interrupt Log Buffer, however, it is quite easy to derive the command word Tx/Rx bit and subaddress or mode code

number from the interrupt log's Interrupt Address Word (IAW) and in most cases, this is sufficient for message identity. If word count, it is available in the MIW.

An alternative option, if the user needs the command word, uses the HI-613x as a multi-terminal device supporting Bus Monitor (SMT) terminal mode concurrently with RT mode. Even if not using the device officially as a monitor, all of the hardware features of the monitor are available to the host on an "as needed" basis. The monitor independent state machine does not slow down RT hardware in any way. The SMT saves message data including command words, in a host accessible circular buffer.

# 10 PSEUDO CODE EXAMPLE

Table 6 shows the programming steps necessary to configure the Holt RT based on the example configuration. The location, Address, and value written/read is provided along with a description of what is being configured in each line. A similar example is shown in the DDC Enhanced Mini-ACE User's Guide Volume 1 - Architectural Reference. These two examples can be examined in detail to show the similarities and differences.

**Table 6 - Holt Pseudo Code Configuration Example**

| Location | Address | Read/Write | Value | Comments |
|---|---|---|---|---|
| Issue Hardware Master Reset | | | | |
| Master Configuration Register | 0x0000 | Write | 0x0048 | The baseline initial value is 0x0048 which enables your selections:<br>* RT1 enabled (or RT1 and RT2 enabled, if a dual-RT project)<br>* Whether mode code 4 & 20 bus shutdowns are Tx-only, or both Rx & Tx. |
| RT1 Configuration Register | 0x0017 | Write | 0x81F0 | The baseline initial value is 0x81F0 which enables your selections:<br>* Broadcast commands including Notice 2 option for segregating broadcast data..<br>* SMCP simplified mode code processing option,.<br>* automatic bus shutdown vs. host bus shutdown for mode codes 4,5,20,21..<br>It also selects two more typical RT settings not optioned in this program:.<br>* No response time-out = 58us.<br>* Dynamic bus control is OFF.<br>There are several mode code and other options that may require changing the baseline register load value provided above. |
| RT1 Operational Status Register | 0x0018 | Write | 0x3800 | Set RT Address to 7. Parity bit = 0 |
| Time Tag Counter Configuration Register | 0x0039 | Write | 0x0007 | Enable internal 64us Time Tag Clock |
| Hardware Interrupt Enable Register | 0x000F | Write | 0x7018 | Loop test failure A |
| Hardware Interrupt Output Enable Register | 0x0013 | Write | 0x7018 | Loop test failure A |
| RT1 Descriptor Base Address Register | 0x0019 | N/A | 0x0400 | Note: This program uses the post-reset default location 0x0400. No write necessary. |
| RT1/RT2 Interrupt Enable Register | 0x0012 | Write | 0x00F0 | The baseline initial value is 0x00F0 which enables:<br>* RT1 IWA (when accessed) interrupt (interrupt every occurrence)<br>* RT1 IXEQZ (index decrements from 1 to zero) interrupt<br>* RT1 IBR IBR (broadcast received) interrupt<br>There are 3 more optionally enabled interrupts; adjust register value if used:<br>* Mode Code 8 (reset RT) interrupt<br>* Message Error interrupt<br>* Illegal Command interrupt (if using Illegal Command Detection) |

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| RT1/RT2 Interrupt Output Enable Register | 0x0016 | Write | 0x00F0 | The baseline initial value is 0x00F0 which enables:<br>* RT1 IWA (when accessed) interrupt (interrupt every occurrence)<br>* RT1 IXEQZ (index decrements from 1 to zero) interrupt<br>* RT1 IBR (broadcast received) interrupt<br>There are 3 more optionally enabled interrupts; adjust register value if used:<br>* Mode Code 8 (reset RT) interrupt<br>* Message Error interrupt<br>* Illegal Command interrupt (if using Illegal Command Detection) |
| Command Illegalization Table | 0x0200 | Write | 0xFFFF | Subaddress 0, broadcast receive mode codes. Only Synchronize (with data) is legal. |
| Command Illegalization Table | 0x0201 | Write | 0xFFFD | |
| Command Illegalization Table | 0x0202-0x020D | Write | 0xFFFF | Broadcast receive subaddress 1-6 illegal |
| Command Illegalization Table | 0x020E-0x020F | Write | 0x0000 | Broadcast receive subaddress 7 legal |
| Command Illegalization Table | 0x0210-0x0225 | Write | 0xFFFF | Broadcast receive subaddress 8-18 illegal |
| Command Illegalization Table | 0x0226-0x0227 | Write | 0x0000 | Broadcast receive subaddress 19 legal |
| Command Illegalization Table | 0x0228-0x023B | Write | 0xFFFF | Broadcast receive subaddress 20-29 illegal |
| Command Illegalization Table | 0x023C-0x023D | Write | 0x0000 | Broadcast receive subaddress 30 legal |
| Command Illegalization Table | 0x023E | Write | 0xFFFF | Subaddress 31, broadcast receive mode codes. Only Synchronize (with data) is legal. |
| Command Illegalization Table | 0x023F | Write | 0xFFFD | |
| Command Illegalization Table | 0x0240 | Write | 0xFE05 | Subaddress 0, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal. |
| Command Illegalization Table | 0x0241 | Write | 0xFFFF | |
| Command Illegalization Table | 0x0242-0x027D | Write | 0xXXXX | Don't need to program (non-mode code broadcast transmit commands) |
| Command Illegalization Table | 0x027E | Write | 0xFF05 | Subaddress 31, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal. |
| Command Illegalization Table | 0x027F | Write | 0xFFFF | |
| Command Illegalization Table | 0x0280 | Write | 0xFFFF | Subaddress 0, non-broadcast receive mode codes. Only Synchronize (with data) is legal. |
| Command Illegalization Table | 0x0281 | Write | 0xFFFD | |
| Command Illegalization Table | 0x0282-0x028D | Write | 0xFFFF | Nonbroadcast subaddresses 1-6 illegal. |
| Command Illegalization Table | 0x028E-0x028F | Write | 0x0000 | Receive subaddress 7 legal |
| Command Illegalization Table | 0x0290-0x02A5 | Write | 0xFFFF | Nonbroadcast receive subaddresses 8-18 illegal. |
| Command Illegalization Table | 0x02A6-0x02A7 | Write | 0x0000 | Nonbroadcast receive subaddress 19 legal |
| Command Illegalization Table | 0x02A8-0x02BB | Write | 0xFFFF | Nonbroadcast subaddresses 1-6 illegal. |
| Command Illegalization Table | 0x02BC-0x02BD | Write | 0x0000 | Receive subaddress 30 legal |

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| Command Illegalization Table | 0x02BE | Write | 0xFFFF | Subaddress 31, non-broadcast receive mode codes. Only Synchronize (with data) is legal. |
| Command Illegalization Table | 0x02BF | Write | 0xFFFD | |
| Command Illegalization Table | 0x02C0 | Write | 0xFE00 | Subaddress 0, non-broadcast transmit mode codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit |
| Command Illegalization Table | 0x02C1 | Write | 0xFFF2 | |
| Command Illegalization Table | 0x02C2-0x02C3 | Write | 0x0000 | Nonbroadcast transmit subaddress 1 legal |
| Command Illegalization Table | 0x02C4-0x02FB | Write | 0xFFFF | Nonbroadcast transmit subaddresses 2-29 illegal |
| Command Illegalization Table | 0x02FC-0x02FD | Write | 0x0000 | Transmit subaddress 30 legal |
| Command Illegalization Table | 0x02FE | Write | 0xFE00 | Subaddress 31, non-broadcast transmit mode codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word are legal. |
| Command Illegalization Table | 0x02FF | Write | 0xFFF2 | |
| RT1 Descriptor Table - Rx SA Quadrant | 0x0400-0x041B | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Rx SA Quadrant | 0x041C | Write | 0x8062 | Rx SA7 Control Word - 1024 word Circular-2 Buffer |
| RT1 Descriptor Table - Rx SA Quadrant | 0x041D | Write | 0x08CC | Rx SA7 Data Block Start Pointer |
| RT1 Descriptor Table - Rx SA Quadrant | 0x041E | Write | 0x08CC | Rx SA7 Data Block Current Pointer |
| RT1 Descriptor Table - Rx SA Quadrant | 0x041F | Write | 0x0D00 | RX SA7 Message Info Buffer Pointer |
| RT1 Descriptor Table - Rx SA Quadrant | 0x0420-0x044B | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Rx SA Quadrant | 0x044C | Write | 0x4004 | Rx SA19 Ping-Pong Buffer Mode |
| RT1 Descriptor Table - Rx SA Quadrant | 0x044D | Write | 0x0866 | Data Pointer A |
| RT1 Descriptor Table - Rx SA Quadrant | 0x044E | Write | 0x0888 | Data Pointer B |
| RT1 Descriptor Table - Rx SA Quadrant | 0x044F | Write | 0x08AA | Broadcast Pointer |
| RT1 Descriptor Table - Rx SA Quadrant | 0x0450-0x0477 | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Rx SA Quadrant | 0x0478 | Write | 0x0000 | Rx SA30 - Control Word - Index 0 Single Buffer 34 words d-wraparound |
| RT1 Descriptor Table - Rx SA Quadrant | 0x0479 | Write | 0x0844 | Rx SA30 - Single Buffer Data Pointer A (34 Words MIW+TTW+Data) |
| RT1 Descriptor Table - Rx SA Quadrant | 0x047A | Write | 0x0000 | Rx SA30 30INDX Index Word - Set to 0 for single buffer mode |
| RT1 Descriptor Table - Rx SA Quadrant | 0x047B | Write | 0x0844 | Rx SA30Broadcast Data Pointer - uses same buffer @ 0x0544 |
| RT1 Descriptor Table - Rx SA Quadrant | 0x047C-0x047F | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Tx SA Quadrant | 0x0480x0483 | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Tx SA Quadrant | 0x0484 | Write | 0x0800 | Tx SA 1 - Index 0 Single Buffer Control Word |
| RT1 Descriptor Table - Tx SA Quadrant | 0x0485 | Write | 0x0822 | Tx SA 1 - Single Buffer Data Pointer A (34 Words MIW+TTW+Data) |

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|---|---|---|---|---|
| RT1 Descriptor Table - Tx SA Quadrant | 0x0486 | Write | 0x0000 | Tx SA 1 INDX Index Word - Set to 0 for single buffer mode |
| RT1 Descriptor Table - Tx SA Quadrant | 0x0487 | Write | 0x0800 | Tx SA 1 Broadcast Data Pointer - Broadcast shares bit bucket @ 0x0500 (34 words) |
| RT1 Descriptor Table - Tx SA Quadrant | 0x0488-0x04F7 | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Tx SA Quadrant | 0x04F8 | Write | 0x0000 | Tx SA 30 - Control Word - Index 0 Single Buffer 34 word d-wraparound |
| RT1 Descriptor Table - Tx SA Quadrant | 0x04F9 | Write | 0x0844 | Tx SA 30 - Single Buffer Data Pointer A (34 Words MIW+TTW+Data) |
| RT1 Descriptor Table - Tx SA Quadrant | 0x04FA | Write | 0x0000 | Tx SA 30 INDX Index Word - Set to 0 for single buffer mode |
| RT1 Descriptor Table - Tx SA Quadrant | 0x04FB | Write | 0x0800 | Tx SA 30 Broadcast Data Pointer - Broadcast shares bit bucket @ 0x0500 (34 words) |
| RT1 Descriptor Table - Tx SA Quadrant | 0x04FC-0x04FF | Write | 0x0000 | Initialize Descriptor Table values to 0x0000 |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0500-0x0543 | Write | 0x0000 | Initialize Descriptor Table Values to 0x0000 - Rx Mode codes |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0544 | Write | 0x6000 | Rx Mode Code 17 - Synchronize w/ Data Control Word (IWA + IWB Interrupts) |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0545 | Write | 0x0000 | Rx Mode Code 17 - MIW |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0546 | Write | 0x0000 | Rx Mode Code 17 - TTW |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0547 | Write | 0x0000 | Rx Mode Code 17 - Data Word (Simplified Mode Command Processing) |
| RT1 Descriptor Table - Rx Mode Code Quadrant | 0x0548-0x057F | Write | 0x0000 | Initialize Descriptor Table Values to 0x0000 - Rx Mode codes |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0580-0x0583 | Write | 0x0000 | Tx Mode Code 0 - Dynamic Bus Control - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0584 | Write | 0x6000 | Tx Mode Code 1 - Synchronize without Data - Control Word (IWA + IWB Interrupts) |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0585 | Write | 0x0000 | Tx Mode Code 1 - MIW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0586 | Write | 0x0000 | Tx Mode Code 1 - TTW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0587 | Write | 0x0000 | Tx Mode Code 1 - Data Word (N/A for Mode code 1) |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0588-0x058B | Write | 0x0000 | Tx Mode Code 2 - Transmit Status Word - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x058C | Write | 0x6000 | Tx Mode Code 3 - Initiate Self Test - Control Word (IWA + IWB Interrupts) |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x058D | Write | 0x0000 | Tx Mode Code 3 - MIW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x058E | Write | 0x0000 | Tx Mode Code 3 - TTW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x058F | Write | 0x0000 | Tx Mode Code 3 - Data Word (N/A for Mode code 3) |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0590-0x0593 | Write | 0x0000 | Tx Mode Code 4 - Transmitter Shutdown - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0594-0x0597 | Write | 0x0000 | Tx Mode Code 5 - Override Transmitter Shutdown - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x0598-0x059B | Write | 0x0000 | Tx Mode Code 6 - Inhibit Terminal Flag - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x059C-0x059F | Write | 0x0000 | Tx Mode Code 7 - Override Inhibit Terminal Flag - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05A0 | Write | 0x6000 | Tx Mode Code 8 - Reset Remote Terminal - Control Word (IWA + IWB Interrupts) |

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| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05A1 | Write | 0x0000 | Tx Mode Code 8 - MIW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05A2 | Write | 0x0000 | Tx Mode Code 8 - TTW |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05A3 | Write | 0x0000 | Tx Mode Code 8 - Data Word (N/A for Mode code 8) |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05A4-<br>0x05BF | Write | 0x0000 | Initialize Descriptor Table Values to 0x0000 - Rx Mode codes |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05C0-<br>0x05C7 | Write | 0x0000 | Tx Mode Code 16 - Transmit Vector Word - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05C8-<br>0x05CB | Write | 0x0000 | Tx Mode Code 18 - Transmit Last Command - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05CC-<br>0x05CF | Write | 0x0000 | Tx Mode Code 19 - Transmit Built In Test Word - No Interrupts Enabled |
| RT1 Descriptor Table - Tx Mode Code Quadrant | 0x05D0-<br>0x05FF | Write | 0x0000 | Initialize Descriptor Table Values to 0x0000 - Rx Mode codes |
| User Data Buffers | 0x0822 | Write | 0x0000 | Tx SA 1 - MIW - Clear Value |
| User Data Buffers | 0x0823 | Write | 0x0000 | Tx SA 1 - TTW - Clear Value |
| User Data Buffers | 0x0824<br>0x0825<br>0x0826<br>:<br>0x0843 | Write | 0x0000<br>0x0001<br>0x0002<br>:<br>0x001F | TX SA 1 - Data words stored (“walking pattern” 0000 to 001F) to be transmitted |
| User Data Buffers | 0x0800-<br>0x0821 | Write | 0x0000 | Tx Broadcast Bit Bucket Buffer (34 words) Clear |
| User Data Buffers | 0x0844-<br>0x0865 | Write | 0x0000 | Tx SA30 34 Word wrap around buffer (34 words) Clear |
| Master Configuration Register | 0x0000 | Write | 0x0058 | Set RT1STEX bit in Master Configuration Register to Start RT1 Execution |

# 11 Additional Resources

- AN-6130DG - MIL-STD-1553 RT Software Design Guide - Provides a detailed look at Holt RT software sample programs and includes flow charts and code details.
- AN-560 - MIL-STD-1553 Remote Terminal GUI User Guide
- Holt Integrated Circuits MIL-STD-1553 RT Configuration Wizard GUI - Can be used to quickly generate example register map, memory map, descriptor table, and Illegalization table.
- Evaluation Kits are available for most devices that include complete and easy to use demonstration software, documentation, schematics, and Bills of Materials. Versions are available with low level sample software and API level software.
- HI-6130 / HI-6131 / HI-6132 MIL-STD-1553 / MIL-STD-1760 3.3V BC / MT / RT Multi-Terminal Device Datasheet
- MAMBA$^{TM}$: HI-6135 3.3V MIL-STD-1553 / MIL-STD-1760 Compact Remote Terminal with SPI Host Interface Datasheet

# 12 Revision History

| Revision | Date | Description of Change |
|---|---|---|
| AN-570, Rev. New | 08/26/15 | Initial Release |