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# HI-8475 ARINC 429 Receiver With parallel and serial outputs Evaluation Board

## Quick Start Guide

Nov 7, 2013

## INTRODUCTION

The Holt HI-8475 Evaluation Board demonstrates features of the HI-8475 ARINC 429 receiver IC. This device will decode 32 bit ARINC 429 words into parallel or serial format without the use of any software. The board and the HI-8475 can be run from a single 3.3V+/- 5% supply voltage. The HI-8475 and EVM (Evaluation Module) requires no software for control; all functions are set by hardware switches. Data can be filtered according to the label content of the ARINC word, using the LLA and FILT input setting and set with DIP switches. Other DIP switches configure the device speed, test modes etc. The EVM is shown in the picture below:

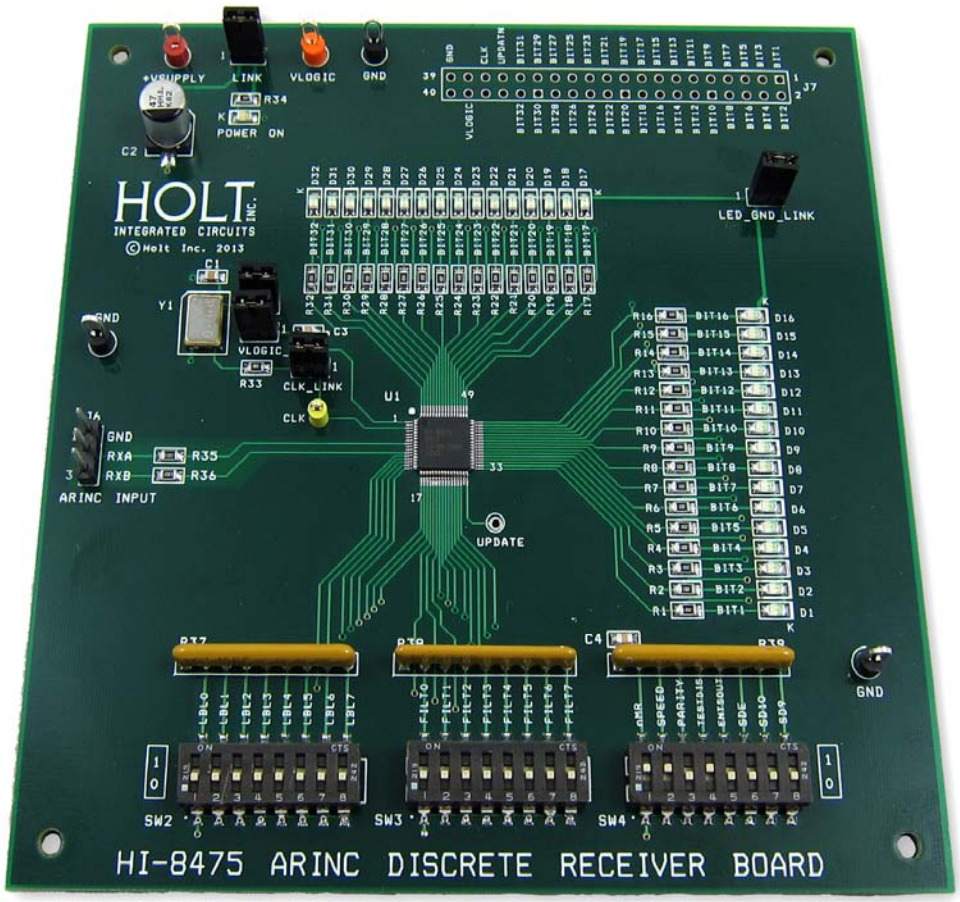


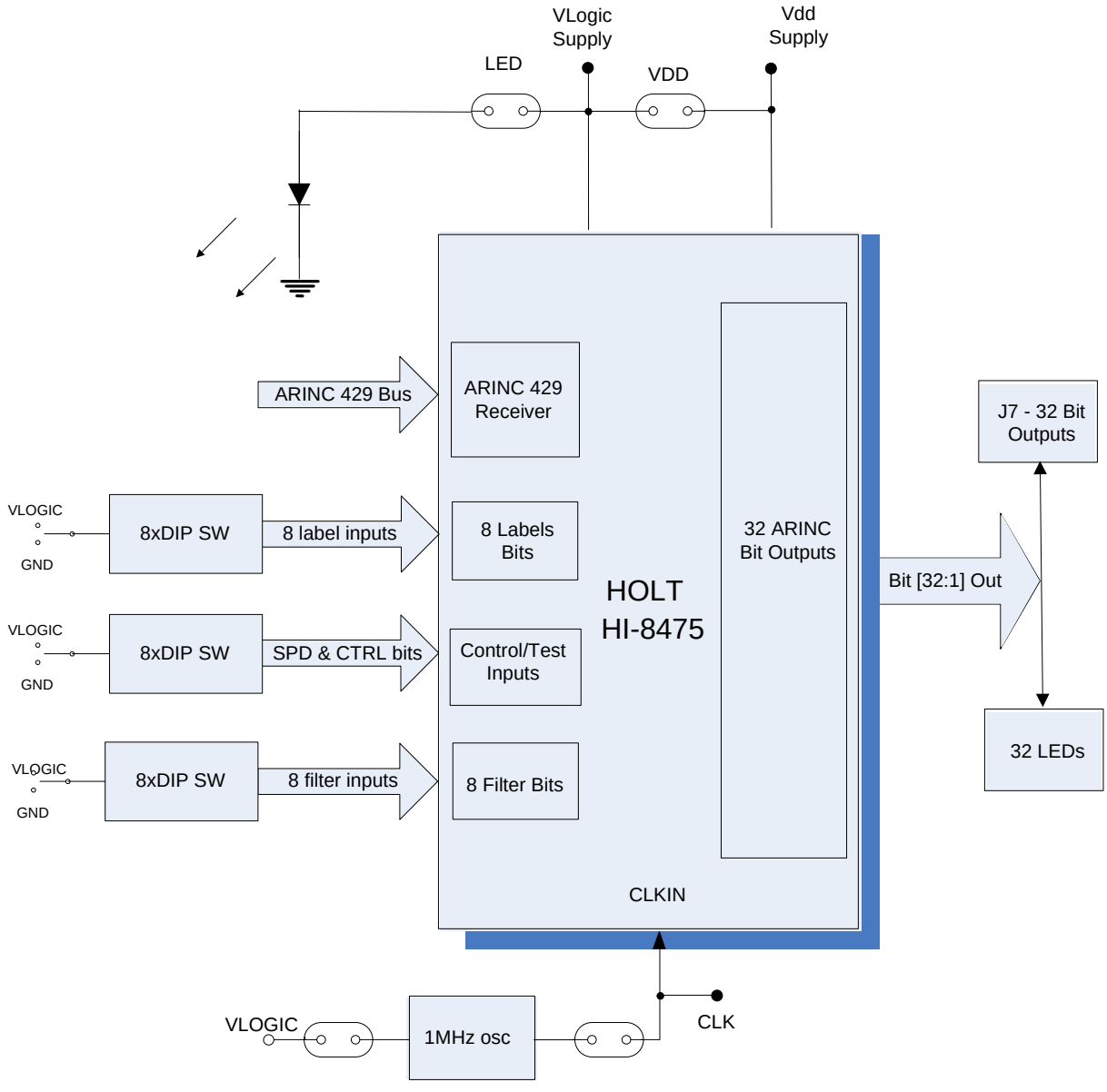

**Fig 1 – HI-8475 Evaluation Board**

This guide summarizes how to get set up and running quickly.

## KIT CONTENTS

- This User Guide
- HI-8475 Evaluation Board

## Board Block Diagram



## Jumper Functions

| REF | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| J1 | LED_GND_LINK | ON | Link for BIT LED current to ground |
| J2 | - | ON | Supplies 3.3V to the 1MHz crystal oscillator |
| J3 | EXTCLK | ON | To use external clock, disconnect link and apply a VLOGIC level clock to the CLK test point |
| J4 | LINK | ON | Link for supply indicator LED |
| J5 | VLOGIC_LINK | ON | Link for device VDD supply current (this supplies the HI-8475 only) and can be used to measure device current, make sure LED link is OFF |

## Test Point and Connector Functions

| REF | NAME | DESCRIPTION |
|---|---|---|
| TP1 | CLK | Use for external clock connection, disconnect link J3 and apply a VLOGIC level clock CLK |
| TP2/TP5 | GND | Ground Test Point |
| TP3/4 | VSUPPLY/VLOGIC | Connect 3.3 or 5V supply |
| TP6 | UPDATE | Test point for Update signal indicates when ARINC word has been received |
| J7 pins 1-32 | Received Data | ARINC data bits 1-32 respectively |
| J7 pin 35 | CLK | 1 MHz Clock |
| J7 pin 38 | VLOGIC | VLOGIC Supply |
| J7 pin 39,40 | GND | Board Ground |

## Switch Functions

| REF | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| SW2 | LABEL[7:0] | OFF | ARINC 429 label bits 0:7.<br>ON = '1' |
| SW3 | FILT[7:0] | OFF | Supplies 3.3V to the 1MHz crystal oscillator |
| SW4/1 | nMR | ON | Master Reset, switch to OFF to reset |
| SW4/2 | SPEED | ON | ON = High Speed<br>OFF = Low Speed |
| SW4/4 | TESTDIS | ON | ON = Disable Test Mode<br>OFF = Enable Test Mode |
| SW4/5 | ENTSTOUT | OFF | ON = Enables Test Output<br>OFF = Enable Test Mode |
| SW4/6 | SDE | OFF | ON = Enables SD bit checking<br>OFF = Disables SD bit checking |
| SW4/7 | SD9 | OFF | ON = Check for SD9 bit = 1<br>OFF = Check for SD9 bit = 0 |
| SW4/8 | SD10 | OFF | ON = Check for SD10 bit = 1<br>OFF = Check for SD10 bit = 0 |

## Using the Board

1. Check all the link and switch positions comply with the tables above. Connect a 3.3V supply to the VLOGIC test point, verify the 'Power On LED' is lit; the board should take about 35mA. The jumper J4 supplies only the Power LED, disconnect if you don't want the LED powered.

2. To measure the device's VLOGIC supply current; remove the VLOGIC_LINK jumper and connect an ammeter across the jumper pins. This point measures only the device current and not the other circuitry on the board, but will include the BIT LEDs current, so also remove jumper LED_GND_LNK .

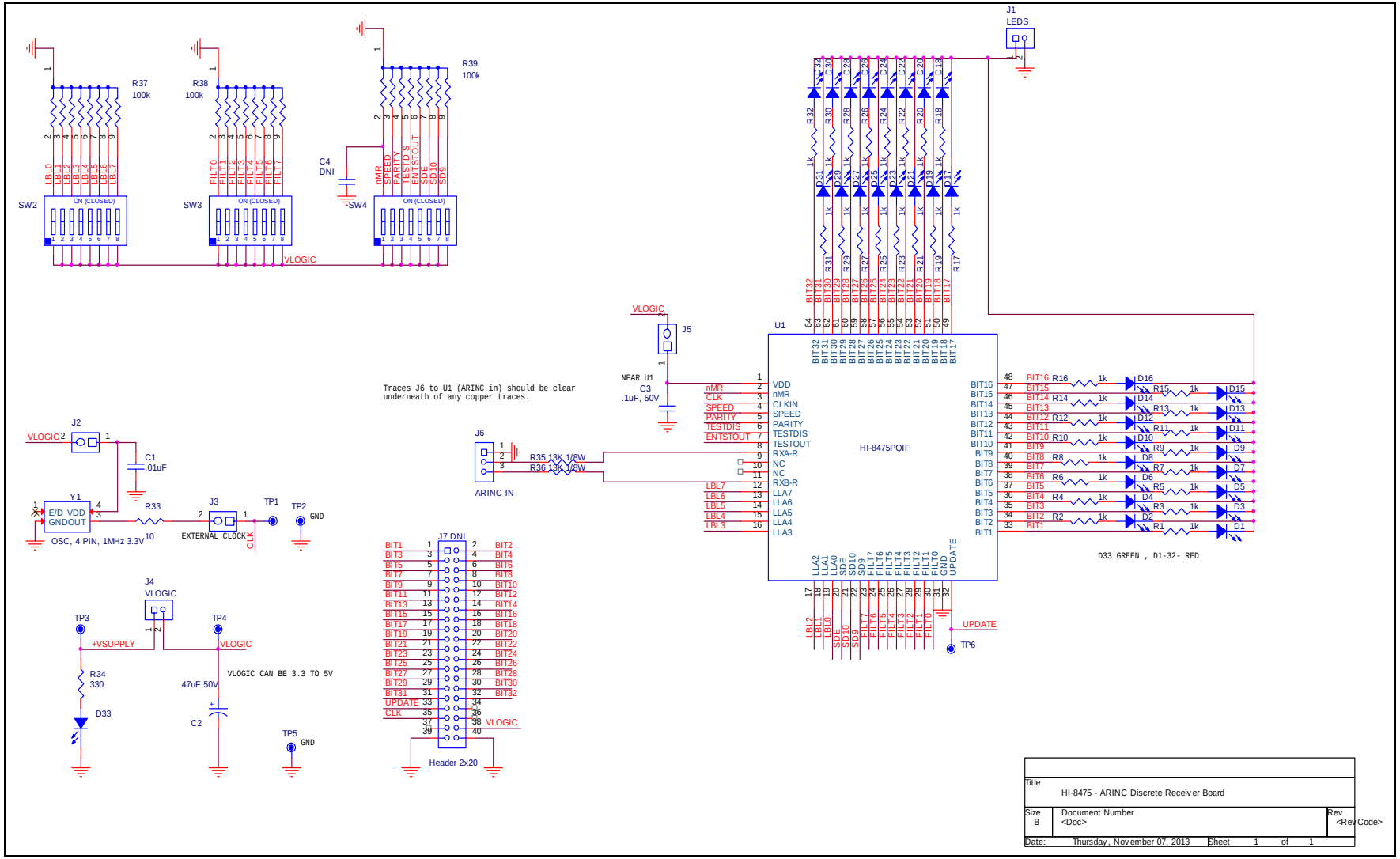
3. The HI-8475 has a Self Test mode. This sends an internal ARINC data stream with all the data bits set to a '1'. The label bits match the settings on the LLA inputs. Set the LBL7:0 and ENTSTOUT switches to '1', set 'TESTDIS' to '0'. Flick the 'nMR' from '1' switch to '0' and back, this causes a reset and the device then initiates the self test sequence; all 1's data should be indicated by all the LED being lit. Return TESTDIS and ENTSTOUT back to default.

4. To test the board an ARINC 429 data source is required; if available the HI-8470 or HI-3593 boards can be used for this. Use a pair of wires to connect the ARINC source + and – to the RXA and RXB terminals respectively on J6. Set the source rate to High Speed 100kb/s; in the default state with all FILT bits set to '0' the device will accept any label value. Transmit an FF FF FF FF pattern and verify all LEDs are lit, repeat with a 00 00 00 00 pattern, all LEDs should go out. With 55 55 55 55 pattern, alternate LEDs should be lit, with the exception of parity bit32.

5. To check the filter bit functions, set the FILT7:0 switches to all '1's. Reset the device, then transmit the 55 55 55 55 pattern again; no data should be received. Now set the LBL switches to '0101 0101' and transmit again; the alternates 1010 pattern should be indicated on the LEDs.

6. Filtering for the SD9 and SD10 ARINC bits can also be done in a similar manner. First put the SDE switch to '1', then set SD9/10 bits as desired.

7. Access to all the ARINC data bits, update and clock is also available on J7, see table for connector pin numbers.


J1
LEDS
U1
HI-8475PQIF
J5
J6
J7 DNI
J2
J3
J4
Y1
SW2
SW3
SW4
R37
100k
R38
100k
R39
100k
C1
.01uF
C2
47uF,50V
C3
.1uF, 50V
C4
DNI
R33
R34
330
R35 13K 1/8W
R36 13K 1/8W
D33
TP1
TP2
TP3
TP4
TP5
TP6
VLOGIC
GND
+VSUPPLY
UPDATE
ARINC IN
EXTERNAL CLOCK
OSC, 4 PIN, 1MHz 3.3V
VLOGIC CAN BE 3.3 TO 5V
Header 2x20
Traces J6 to U1 (ARINC in) should be clear
underneath of any copper traces.
NEAR U1
D33 GREEN , D1-32- RED
Title
HI-8475 - ARINC Discrete Receiver Board
Size
B
Document Number
<Doc>
Rev
<Rev Code>
Date:
Thursday, November 07, 2013
Sheet
1
of
1

| Bill of Materials | | | HI-8475 Arinc Discrete Receiver Board | | 29-Oct-13 |
|---|---|---|---|---|---|
| | | | | | |
| ***Item*** | ***Qty*** | ***Description*** | ***Reference*** | ***DigiKey*** | ***Mfr P/N*** |
| | | | | | |
| 1 | 2 | Capacitor, Cer 0.1uF 20% 50V Z5U 0805 | C3,C4 | 399-1176-1-ND | Kemet C0805C104M5UACTU |
| 2 | 1 | Capacitor, Cer 0.01uF 20% 50V Z5U 0805 | C1 | 399-1160-1-ND | Kemet C0805C103M5RACTU |
| 3 | 1 | Cap Alum 47uF 50V 20% SMD | C2 | PCE4222CT-ND | Panasonic EEE-HA1H470XPS |
| 4 | 1 | Header, Male 1x3, .1" Pitch | J6 | S1012E-03-ND | Sullins S1012E-03-ND |
| 5 | 5 | Header, Male 1x2, .1" Pitch | J1,J2,J3,J4,J5 | S1012E-02-ND | Sullins S1012E-02-ND |
| 6 | 1 | Header, Male 2x20 0.1" Pitch, 0.230" Pins, 0.120" Tail | J7 Optional | S2012E-20-ND | Sullins PEC36DAAN |
| 7 | 1 | LED Green 0805 | D33 | 160-1179-1-ND | LiteOn LTST-C170GKT |
| 8 | 31 | LED Red 0805 | D1-D32 | 160-1178-1-ND | LiteOn LTST-C170GKT |
| 9 | 1 | Resistor, 10 5% 1/8W 0805 | R33 | P10ACT-ND | Panasonic ERJ-6GEYJ100V |
| 10 | 1 | Resistor, 330 5% 1/8W 0805 | R34 | P330ACT-ND | Panasonic ERJ-6GEYJ331V |
| 11 | 32 | Resistor, 1.0K 5% 1/8W 0805 | R1-R32 | P1.0KACT-ND | Panasonic ERJ-6GEYJ102V |
| 12 | 4 | Resistor, 3.6K 5% 1/8W 0805 | R1,R12,R14,R25 | P3.6KACT-ND | Panasonic ERJ-6GEYJ362V |
| 13 | 2 | Resistor, 13K 5% 1/8W 0805 | R35,R36 | P13KACT-ND | Panasonic ERJ-6GEYJ133V |
| 14 | 3 | Resistor Network, 100K 5% 8 Res 9SIP | R37,R38,R39 | 4609X-101-104LF-ND | Bourns 4609X-101-104LF |
| 15 | 1 | Osc 1.MHz 3.3V, 5x7mm SMD | Y1 | 631-1122-1-ND | FOX FXO-HC735-1 |
| 16 | 3 | Switch Tape Seal 8Pos SMD | SW2,SW3,SW4 | CT2198MST-ND | CTS 219-8MST |
| 17 | 1 | Test Point, Red Insulator, 0.062" hole | TP3 | 5010K-ND | Keystone 5010 |
| 18 | 3 | Test Point, Black Insulator, 0.062" hole | TP2,TP5,TP7 | 5011K-ND | Keystone 5011 |
| 19 | 1 | Test Point, White Insulator, 0.062" hole | TP1 | 5012K-ND | Keystone 5012 |
| 20 | 1 | Test Point, Orange Insulator, 0.062" hole | TP4 | 5013K-ND | Keystone 5013 |
| 21 | 1 | Test Point, Yellow Insulator, 0.062" hole | TP6 | 5014K-ND | Keystone 5014 |
| 22 | 1 | HI-8475 - 64TQFP | U1 | HOLT IC | Holt IC |
| 23 | 5 | 3M Bumpon | Each corner and center. | SJ5746-0-ND | 3M: SJ61A1 |

# Appendix 1 Lightning Protection

The ARINC 429 inputs (RXA-R and RXB-R) are protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) when used with the recommended 13kohm series input resistors. For more details please see the latest datasheet.

The level of lightning protection can be increased by using external components, please see the Application Notes available on Holt's website http://www.holtic.com.

The layout of a HI-8475 board should always have low conductivity paths from the device power/ground pin to the relevant power or ground origin. These paths should avoid proximity to sense or other signal traces; this applies to above and below as well as horizontally. It is good practice to have a power and ground 'moat' beneath the sense line to prevent disturbance on these lines during a 'lightning' event.

## REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| QSG-8475, Rev. New | 11-07-13 | Initial Release |
| | | |
| | | |
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