HI-8475, HI-8476

Self-contained ARINC 429 Receiver / Decoder

November 2014

DESCRIPTION

The HI-8475 is an ARINC 429 Receiver IC, designed for applications where an MCU is not desired or otherwise required. The device does not require an MCU for programmed configuration or operation. It is fully configured using control input pins, greatly simplifying system qualification.

The 64-pin HI-8475 receives ARINC 429 data directly from the bus and makes the data available at 32 digital output pins. ARINC 429 label filtering is defined by 16 digital input pins, defining a maskable label match to enable reception of a single label or group of labels.

The 128-pin HI-8476 option increases the label match capability by two maskable labels, and provides both true and complementary digital outputs to simplify external logic, or set a default post-reset condition for downstream circuits, before a first ARINC 429 word is received.

The receiver inputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) with the use of only two external resistors.

A single 1 MHz clock source is required for ARINC 429 bit timing. The device supports both high-speed and low-speed ARINC 429 data rates.

The HI-8475 operates from a single 3.3V or 5.0V power supply.

FEATURES

- Pin programmable - **requires no MCU or software control**
- No need for certification to RTCA DO-178B, "Software Considerations in Airborne Systems and Equipment"
- Robust CMOS Silicon-on-Insulator (SOI) technology
- On-chip ARINC 429 Line Receiver
- 3.3 V or 5V single supply operation
- Maskable Label Filtering for single label or groups of labels
- Internal lightning protection circuitry for receiver inputs allows compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Tests using only two external resistors.
- 128-pin HI-8476 option provides enhanced label filtering and output flexibility
- Certifiable to RTCA DO-254, "Design Assurance for Airborne Electronic Hardware"

TYPICAL APPLICATION

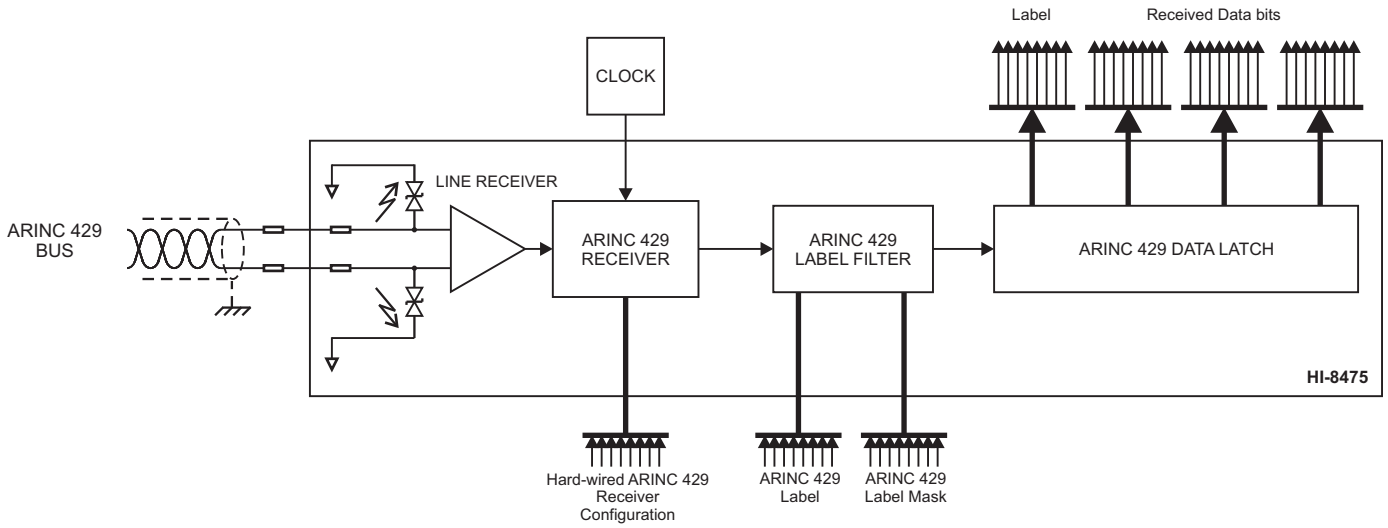


Figure 1

BLOCK DIAGRAM

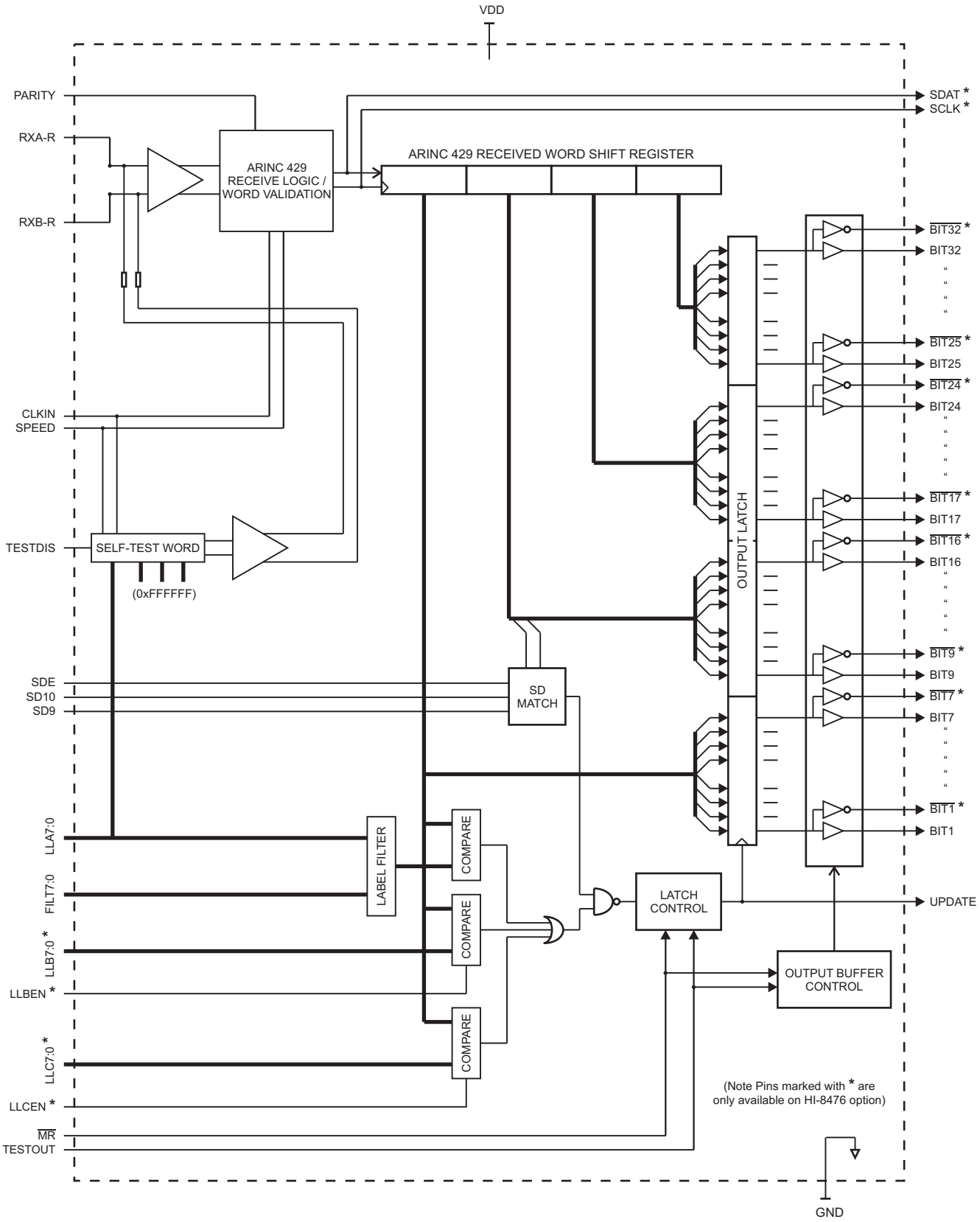


Figure 2

PIN DESCRIPTIONS

SYMBOL	HI-8475 PIN	HI-8476 PIN	FUNCTION	DESCRIPTION
VDD	1	1	Supply	3.3V or 5.0V power
$\overline{MR}$	2	2	Digital Input	Master Reset. Active low. Clears the output latch and initializes the ARINC receiver logic
CLKIN	3	3	Digital Input	1 MHz (+/- 1%) must be provided to operate the ARINC429 receiver
SPEED	4	4	Digital Input	If high ARINC 429 receiver set for 100 kbs, else 12.5 kbs
PARITY	5	5	Digital Input	If high, enables odd parity checking of incoming ARINC 429 words
SCLK	N/A	6	Digital Output	Received data clock. May be used to clock received ARINC 429 word into external shift register
SDAT	N/A	7	Digital Output	ARINC 429 received data out. May be shifted into an external shift register using SCLK
TESTDIS	6	8	Digital Input	Initiates internal self-test routine following Master Reset when tied low
TESTOUT	7	9	Digital Input	If high, allows self-test word to be output on BIT(1:32) pins at end of self-test routine
RXA-R	8	11	Analog Input	Positive connection to ARINC 429 bus. Used with external 13kΩ resistor.
RXB-R	11	18	Analog Input	Negative connection to ARINC 429 bus. Used with external 13kΩ resistor.
LLBEN	N/A	20	Digital Input	When high enables label matching for LLB(7:0) inputs
LLCEN	N/A	21	Digital Input	When high enables label matching for LLC(7:0) inputs
LLB7	N/A	22	Digital Input	Label B match bit 7. Compared to ARINC 429 bit 1 if LLBEN is high
LLA7	12	23	Digital Input	Label A match bit 7. Compared to ARINC 429 bit 1 when unmasked by FILT7
LLB6	N/A	24	Digital Input	Label B match bit 6. Compared to ARINC 429 bit 2 if LLBEN is high
LLA6	13	25	Digital Input	Label A match bit 6. Compared to ARINC 429 bit 2 when unmasked by FILT6
LLB5	N/A	26	Digital Input	Label B match bit 5. Compared to ARINC 429 bit 3 if LLBEN is high
LLA5	14	27	Digital Input	Label A match bit 5. Compared to ARINC 429 bit 3 when unmasked by FILT5
LLB4	N/A	28	Digital Input	Label B match bit 4. Compared to ARINC 429 bit 4 if LLBEN is high
LLA4	15	29	Digital Input	Label A match bit 4. Compared to ARINC 429 bit 4 when unmasked by FILT4
LLB3	N/A	30	Digital Input	Label B match bit 3. Compared to ARINC 429 bit 5 if LLBEN is high
LLA3	16	31	Digital Input	Label A match bit 3. Compared to ARINC 429 bit 5 when unmasked by FILT3
LLB2	N/A	32	Digital Input	Label B match bit 2. Compared to ARINC 429 bit 6 if LLBEN is high
LLA2	17	36	Digital Input	Label A match bit 2. Compared to ARINC 429 bit 6 when unmasked by FILT2
LLB1	N/A	37	Digital Input	Label B match bit 1. Compared to ARINC 429 bit 7 if LLBEN is high
LLA1	18	38	Digital Input	Label A match bit 1. Compared to ARINC 429 bit 7 when unmasked by FILT1
LLB0	N/A	39	Digital Input	Label B match bit 0. Compared to ARINC 429 bit 8 if LLBEN is high
LLA0	19	40	Digital Input	Label A match bit 0. Compared to ARINC 429 bit 8 when unmasked by FILT0
SDE	20	41	Digital Input	When high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance
SD10	21	42	Digital Input	If SDE is high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance
SD9	22	43	Digital Input	If SDE is high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance
LLC7	N/A	44	Digital Input	Label C match bit 7. Compared to ARINC 429 bit 1 if LLCEN is high
FILT7	23	45	Digital Input	If high, ARINC 429 bit 1 is enabled for label match comparison, else ignore state of ARINC429 bit 1
LLC6	N/A	46	Digital Input	Label C match bit 6. Compared to ARINC 429 bit 2 if LLCEN is high
FILT6	24	47	Digital Input	If high, ARINC 429 bit 2 is enabled for label match comparison, else ignore state of ARINC429 bit 2
LLC5	N/A	48	Digital Input	Label C match bit 5. Compared to ARINC 429 bit 3 if LLCEN is high
FILT5	25	49	Digital Input	If high, ARINC 429 bit 3 is enabled for label match comparison, else ignore state of ARINC429 bit 3
LLC4	N/A	50	Digital Input	Label C match bit 4. Compared to ARINC 429 bit 4 if LLCEN is high
FILT4	26	51	Digital Input	If high, ARINC 429 bit 4 is enabled for label match comparison, else ignore state of ARINC429 bit 4
LLC3	N/A	52	Digital Input	Label C match bit 3. Compared to ARINC 429 bit 5 if LLCEN is high
FILT3	27	53	Digital Input	If high, ARINC 429 bit 5 is enabled for label match comparison, else ignore state of ARINC429 bit 5
LLC2	N/A	54	Digital Input	Label C match bit 2. Compared to ARINC 429 bit 6 if LLCEN is high
FILT2	28	55	Digital Input	If high, ARINC 429 bit 6 is enabled for label match comparison, else ignore state of ARINC429 bit 6
LLC1	N/A	56	Digital Input	Label C match bit 1. Compared to ARINC 429 bit 7 if LLCEN is high
FILT1	29	57	Digital Input	If high, ARINC 429 bit 7 is enabled for label match comparison, else ignore state of ARINC429 bit 7
LLC0	N/A	58	Digital Input	Label C match bit 0. Compared to ARINC 429 bit 8 if LLCEN is high
FILT0	30	59	Digital Input	If high, ARINC 429 bit 8 is enabled for label match comparison, else ignore state of ARINC429 bit 8
GND	31	60	Supply	0V supply pin
UPDATE	32	61	Digital Output	Transitions high when a new word is transferred to the output latch and remains high until the next (new) word is transferred.

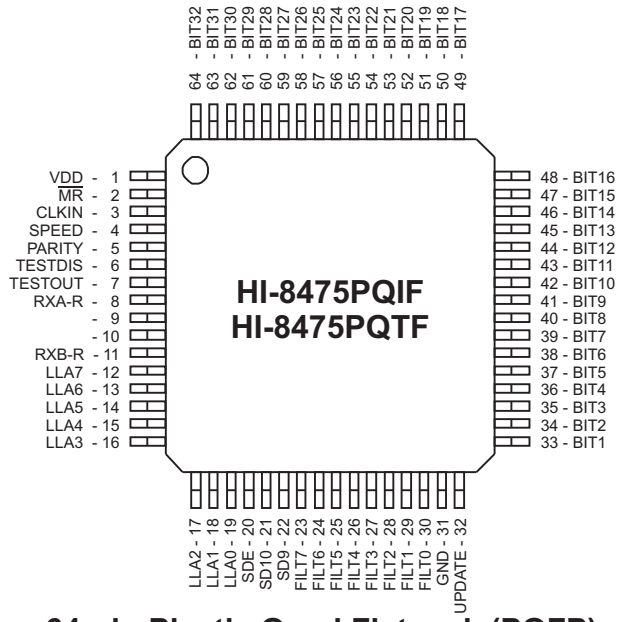
PIN DESCRIPTIONS (cont.)

SYMBOL	HI-8475 PIN	HI-8476 PIN	FUNCTION	DESCRIPTION
$\overline{\text{BIT1}}$	N/A	65	Digital Output	ARINC 429 bit 1 inverted output from qualified received word, updated on UPDATE rising edge
BIT1	33	66	Digital Output	ARINC 429 bit 1 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT2}}$	N/A	67	Digital Output	ARINC 429 bit 2 inverted output from qualified received word, updated on UPDATE rising edge
BIT2	34	68	Digital Output	ARINC 429 bit 2 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT3}}$	N/A	69	Digital Output	ARINC 429 bit 3 inverted output from qualified received word, updated on UPDATE rising edge
BIT3	35	70	Digital Output	ARINC 429 bit 3 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT4}}$	N/A	71	Digital Output	ARINC 429 bit 4 inverted output from qualified received word, updated on UPDATE rising edge
BIT4	36	72	Digital Output	ARINC 429 bit 4 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT5}}$	N/A	73	Digital Output	ARINC 429 bit 5 inverted output from qualified received word, updated on UPDATE rising edge
BIT5	37	74	Digital Output	ARINC 429 bit 5 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT6}}$	N/A	75	Digital Output	ARINC 429 bit 6 inverted output from qualified received word, updated on UPDATE rising edge
BIT6	38	76	Digital Output	ARINC 429 bit 6 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT7}}$	N/A	77	Digital Output	ARINC 429 bit 7 inverted output from qualified received word, updated on UPDATE rising edge
BIT7	39	78	Digital Output	ARINC 429 bit 7 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT8}}$	N/A	79	Digital Output	ARINC 429 bit 8 inverted output from qualified received word, updated on UPDATE rising edge
BIT8	40	80	Digital Output	ARINC 429 bit 8 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT9}}$	N/A	81	Digital Output	ARINC 429 bit 9 inverted output from qualified received word, updated on UPDATE rising edge
BIT9	41	82	Digital Output	ARINC 429 bit 9 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT10}}$	N/A	83	Digital Output	ARINC 429 bit 10 inverted output from qualified received word, updated on UPDATE rising edge
BIT10	42	84	Digital Output	ARINC 429 bit 10 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT11}}$	N/A	85	Digital Output	ARINC 429 bit 11 inverted output from qualified received word, updated on UPDATE rising edge
BIT11	43	86	Digital Output	ARINC 429 bit 11 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT12}}$	N/A	87	Digital Output	ARINC 429 bit 12 inverted output from qualified received word, updated on UPDATE rising edge
BIT12	44	88	Digital Output	ARINC 429 bit 12 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT13}}$	N/A	89	Digital Output	ARINC 429 bit 13 inverted output from qualified received word, updated on UPDATE rising edge
BIT13	45	90	Digital Output	ARINC 429 bit 13 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT14}}$	N/A	91	Digital Output	ARINC 429 bit 14 inverted output from qualified received word, updated on UPDATE rising edge
BIT14	46	92	Digital Output	ARINC 429 bit 14 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT15}}$	N/A	93	Digital Output	ARINC 429 bit 15 inverted output from qualified received word, updated on UPDATE rising edge
BIT15	47	94	Digital Output	ARINC 429 bit 15 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT16}}$	N/A	95	Digital Output	ARINC 429 bit 16 inverted output from qualified received word, updated on UPDATE rising edge
BIT16	48	96	Digital Output	ARINC 429 bit 16 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT17}}$	N/A	97	Digital Output	ARINC 429 bit 17 inverted output from qualified received word, updated on UPDATE rising edge
BIT17	49	98	Digital Output	ARINC 429 bit 17 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT18}}$	N/A	99	Digital Output	ARINC 429 bit 18 inverted output from qualified received word, updated on UPDATE rising edge
BIT18	50	100	Digital Output	ARINC 429 bit 18 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT19}}$	N/A	101	Digital Output	ARINC 429 bit 19 inverted output from qualified received word, updated on UPDATE rising edge
BIT19	51	102	Digital Output	ARINC 429 bit 19 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT20}}$	N/A	103	Digital Output	ARINC 429 bit 20 inverted output from qualified received word, updated on UPDATE rising edge
BIT20	52	104	Digital Output	ARINC 429 bit 20 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT21}}$	N/A	105	Digital Output	ARINC 429 bit 21 inverted output from qualified received word, updated on UPDATE rising edge
BIT21	53	106	Digital Output	ARINC 429 bit 21 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT22}}$	N/A	107	Digital Output	ARINC 429 bit 22 inverted output from qualified received word, updated on UPDATE rising edge
BIT22	54	108	Digital Output	ARINC 429 bit 22 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT23}}$	N/A	109	Digital Output	ARINC 429 bit 23 inverted output from qualified received word, updated on UPDATE rising edge
BIT23	55	110	Digital Output	ARINC 429 bit 23 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT24}}$	N/A	111	Digital Output	ARINC 429 bit 24 inverted output from qualified received word, updated on UPDATE rising edge
BIT24	56	112	Digital Output	ARINC 429 bit 24 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT25}}$	N/A	113	Digital Output	ARINC 429 bit 25 inverted output from qualified received word, updated on UPDATE rising edge
BIT25	57	114	Digital Output	ARINC 429 bit 25 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT26}}$	N/A	115	Digital Output	ARINC 429 bit 26 inverted output from qualified received word, updated on UPDATE rising edge
BIT26	58	116	Digital Output	ARINC 429 bit 26 output from qualified received word, updated on UPDATE rising edge

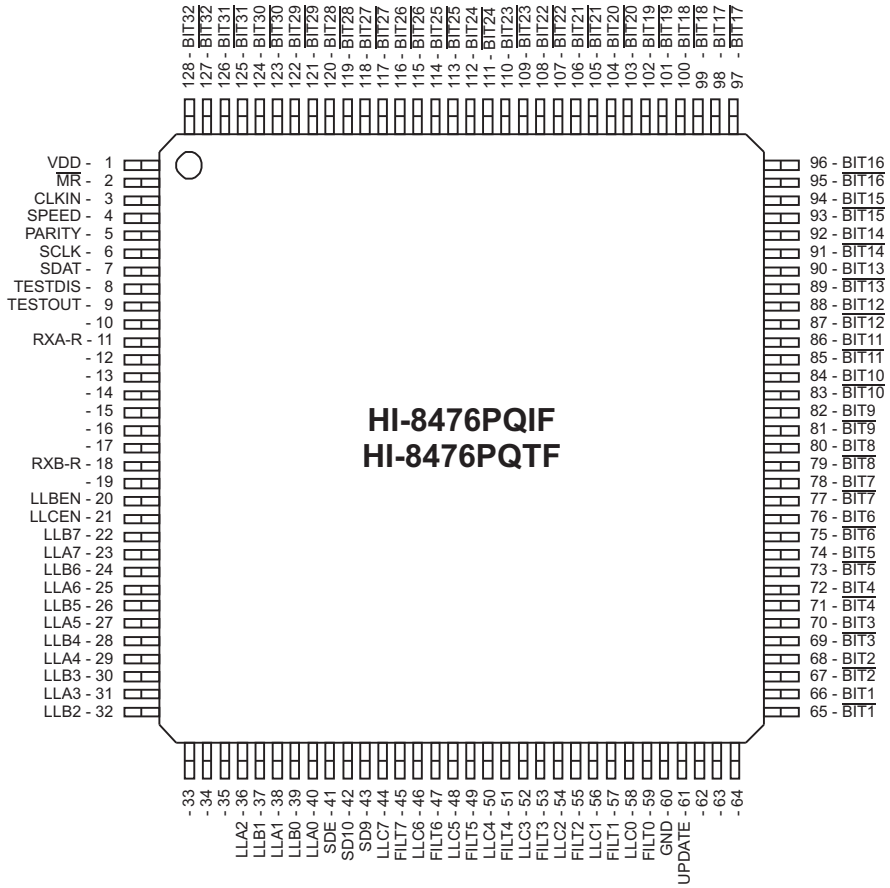
PIN DESCRIPTIONS (cont.)

SYMBOL	HI-8475 PIN	HI-8476 PIN	FUNCTION	DESCRIPTION
$\overline{\text{BIT27}}$	N/A	117	Digital Output	ARINC 429 bit 27 inverted output from qualified received word, updated on UPDATE rising edge
BIT27	59	118	Digital Output	ARINC 429 bit 27 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT28}}$	N/A	119	Digital Output	ARINC 429 bit 28 inverted output from qualified received word, updated on UPDATE rising edge
BIT28	60	120	Digital Output	ARINC 429 bit 28 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT29}}$	N/A	121	Digital Output	ARINC 429 bit 29 inverted output from qualified received word, updated on UPDATE rising edge
BIT29	61	122	Digital Output	ARINC 429 bit 29 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT30}}$	N/A	123	Digital Output	ARINC 429 bit 30 inverted output from qualified received word, updated on UPDATE rising edge
BIT30	62	124	Digital Output	ARINC 429 bit 30 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT31}}$	N/A	125	Digital Output	ARINC 429 bit 31 inverted output from qualified received word, updated on UPDATE rising edge
BIT31	63	126	Digital Output	ARINC 429 bit 31 output from qualified received word, updated on UPDATE rising edge
$\overline{\text{BIT32}}$	N/A	127	Digital Output	BIT32 inverted output.
BIT32	64	128	Digital Output	ARINC 429 bit 32 output from qualified received word, updated on UPDATE rising edge. If PARITY pin is HIGH (parity checking enabled), BIT32 acts as a parity error output (see text).

PIN CONFIGURATIONS



64-pin Plastic Quad Flatpack (PQFP)



128-pin Plastic Quad Flatpack (PQFP)

Figure 3

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8475 and HI-8476 are autonomous ARINC 429 receivers intended for applications where a host MCU is either undesirable or not otherwise needed. The parts contain an on-chip ARINC 429 line receiver and protocol logic to decode and capture selected ARINC 429 data words. The ARINC 429 word is made available to the application on 32 CMOS output pins, which may be used to directly control subsystem functions. The enhanced HI-8476 option provides data in both true and complement form for each bit and has three levels of label filtering. The HI-8476 also provides a clocked serial data output interface to allow the application to monitor all ARINC 429 received words and let them be captured in an external shift register if so desired.

ARINC 429 LINE RECEIVER

An on-chip ARINC 429 analog receiver operates from the same supply as the digital logic. Two input pins, RXA-R and RXB-R, require an external series resistor of 13 kOhm between the pin and ARINC 429 bus for proper signal level detection. With these resistors the inputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection, Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B).

Application Note AN-301 provides guidelines for enhanced lightning protection circuitry.

RESET OPERATION

Applications may wire the device outputs directly to logic, relay drivers, DACs, etc. It is therefore important to define the state of the outputs during the interval between system reset and the reception of a first, valid ARINC 429 word.

The 64-pin HI-8475 holds all BIT1:32 outputs in tri-state following reset. The pins have internal weak (100kOhm) pull-down resistors. This provision allows hardwiring 10kOhm resistors at each output to VDD or GND to set the initial state of the 32 bits.

The 128-pin HI-8476 provides both true and complement outputs for each 32 bit ARINC 429 data word received. This allows the user to select a desired reset state by externally wiring the appropriate bit polarities. Reset forces all Zeros at the true outputs. Wiring a mixture of true and complements presumes the user has control or can work with the coding of subsequent received ARINC 429 words. Note that the tri-state option is not available on the HI-8476.

ARINC 429 WORD DECODER

A 1MHz clock at CLKIN samples the outputs of the ARINC 429 receiver at ten times the nominal bit rate. The SPEED pin should be set to a zero when connecting the HI-8475 to a low-speed (12.5kb/s) ARINC 429 bus, or to a one for connection to a high-speed (100kb/s) bus. The PARITY pin selects whether parity checking of incoming ARINC 429 words is enabled. If the PARITY pin is set high, the receiver logic checks for Odd parity. ARINC bit 32 is overwritten by the HI-8475 to a zero if odd parity was received, or to a one if even parity (error) was received. Regardless of parity error, the word is still stored in the input shift register (see Figure 2). Setting the PARITY pin low disables parity checking and all ARINC 429 received words are passed to the input shift register unaltered.

The SCLK and SDAT output pins on the HI-8476 option follow the clock and data input to the input shift register. The 32 data bits are each valid on the rising edge of SCLK. See the timing diagram section for details.

LABEL FILTERING

All properly encoded ARINC 429 received data words are captured by the input shift register. However, only words meeting user-specified label and S/D values are then passed to the output latch (see Figure 2). Eight label match inputs, LLA:(7:0), and eight filter inputs, FILT(7:0) define the label match criteria. Setting a filter bit high enables matching for that bit of the received ARINC 429 label byte. If FILTn is high, the ARINC label bit must match the value at LLAn for the word to be accepted. Setting FILTn low, disables matching for that bit, declaring it a “don’t care” bit.

Setting FILT(7:0) to 0x00 turns off label matching for all label bits; in this case the HI-8475 accepts all ARINC 429 labels. Judicious selection of LLA(7:0) and FILT(7:0) values allows either a single ARINC 429 label to be accepted by the filter or a group of labels. For example, setting FILT(7:0) to 0xFC and LLA(7:0) to 0x80, accepts ARINC 429 labels 0x80 through 0x83 only (10 - 13 octal).

Note that ARINC 429 defines the label bits as “big-endian”. Therefore received ARINC 429 bit 1 is the MSB (label bit 7), and ARINC received bit 8 is the LSB (label bit 0). Thus LLA7 and FILT7 compare ARINC bit 1, LLA6 and FILT6 compare ARINC bit 2, etc.

ARINC bits 9 and 10 are the SD bits. Incoming ARINC 429 words captured in the input shift register may also be compared for SD matching as a condition for passing to the output latch. Taking the SDE pin high enables this feature. When SDE is high, ARINC bits 9 and 10 are compared with the state of the SD9 and SD10 input pins. Label filtering AND SDE matching criteria must be met to allow a received word to be passed to the output latch.

FUNCTIONAL DESCRIPTION (cont.)

Label filtering is further enhanced on the 128-pin HI-8476 product variant. Three sets of LL pins are provided: LLA(7:0), LLB(7:0) and LLC(7:0). LLB(7:0) label matching is enabled by forcing LLBEN high. Similarly, LLC(7:0) is enabled by LLCEN. The FILT(7:0) pins are not used by LLB(7:0) or LLC(7:0), such that an exact match must occur for label acceptance. Acceptance by any one or more of the LLn/FILT combinations accepts the incoming ARINC 429 word. For example, LLA(7:0)=0x80, LLB(7:0)=0xAA, LLC(7:0)=0xBB and FILT(7:0)=0xFC, accepts ARINC 429 labels 0x80-0x83, 0xAA and 0xBB only.

PARALLEL OUTPUT DATA

Data is passed to the output latch one CLKIN period before the rising edge of the UPDATE pin and remains stable until a new valid and label-matching ARINC 429 word is received. UPDATE goes low as soon as the first bit of a potential new ARINC 429 word is detected by the receiver.

SELF-TEST OPERATION

The HI-8475 includes a self-test feature. See Figure 2. The purpose of the Self-Test word block is to send a test transmission to the Receiver inputs (after the input resistor) coded with LLA followed by all Ones. It is activated by an edge sensitive input. The edge is generated on the first clock (CLKIN pin) after the Master Reset rising edge, only if the TESTDIS input is wired Low. The user has the option of enabling the received self-test word to be latched into the output latch and made available at the BIT(1:32) outputs. If the TESTOUT input is high, the tri-state operation after Master Reset is cancelled one CLKIN period before UPDATE goes high and the test word is output at BIT(1:32). If TESTOUT is low, the BIT(1:32) outputs remain in tri-state until the first valid and matching ARINC 429 word is received. The UPDATE pin stays high until the first bit of a potential new ARINC 429 word is received.

Note that label and SDE filtering apply equally to the self-test word as for normal operation.

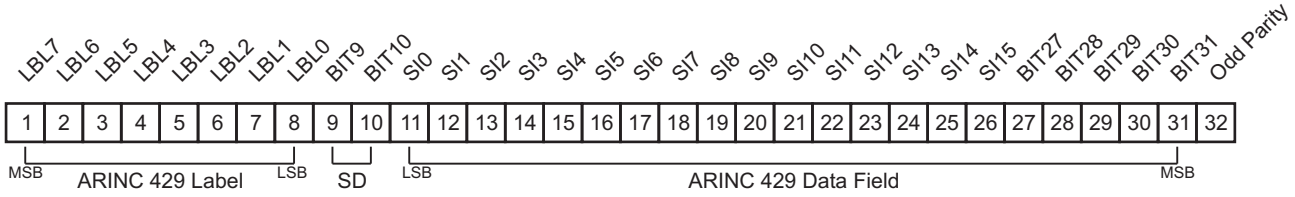


Figure 4. ARINC 429 Word Format

LIGHTNING PROTECTION

The ARINC 429 data bus inputs, RXA and RXB, are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) with the use 13kOhm external resistors. See application notes AN-300 and AN-301 for further details on lightning protection. Figures 5, 6 and 7 summarize the waveforms.

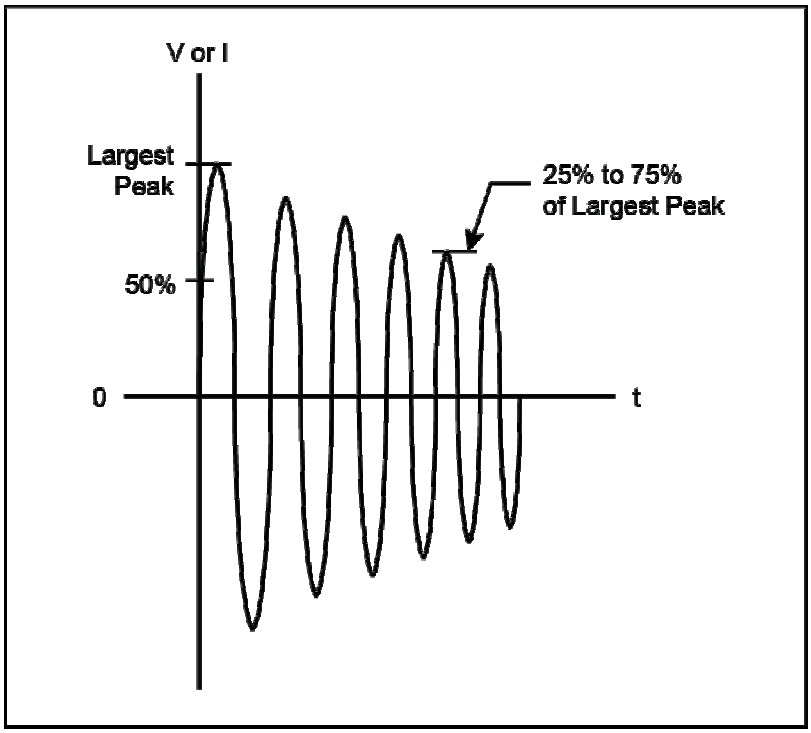


Figure 5. DO-160G Lightning Induced Transient Voltage Waveform 3.
Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4

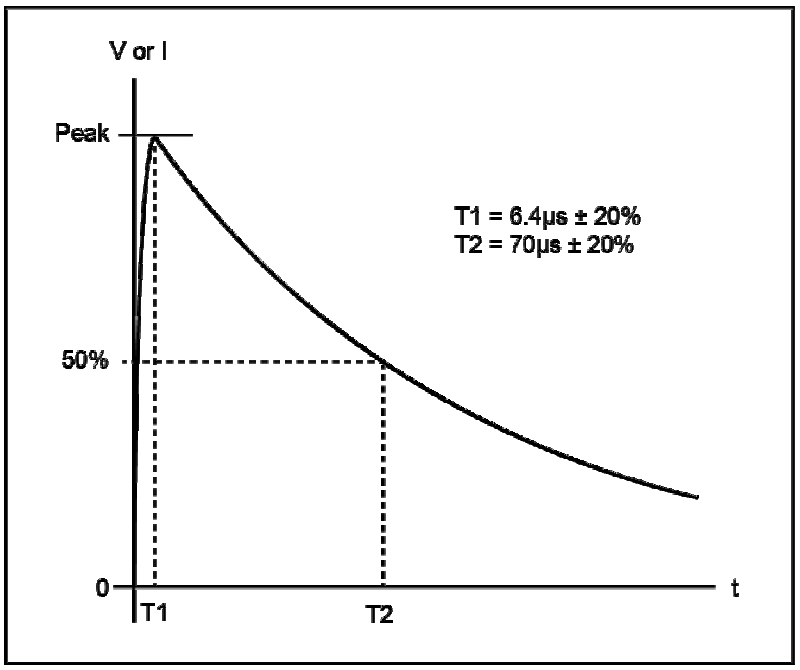


Figure 6. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5

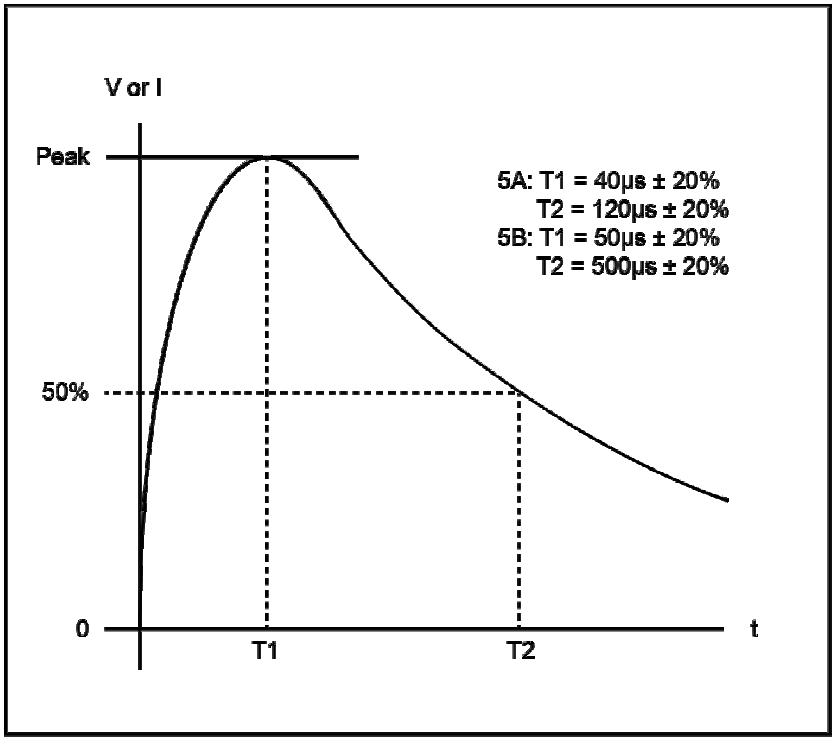


Figure 6. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground
Supply Voltage (VDD) ..... -0.3V to +7V
Maximum Current at any pin ..... -150 mA
Logic Input Voltage Range ..... -0.3V to VLOGIC+0.3V
ARINC 429 Input Voltage Range ..... -120V to +120V
Continuous Power Dissipation (TA=+70°C) (derate 10.0mW/°C above +70°C) 1.5W
Solder Temperature (reflow) ..... 260°C
Junction Temperature ..... 175°C
Storage Temperature ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage VLOGIC ..... 3.0V to 5.5V
Operating Temperature Range Industrial Screening ..... -40°C to +85°C Hi-Temp Screening ..... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

VDD = 3.0 to 5.5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ARINC 429 RECEIVER INPUTS (RXA-R/RXB-R with external 13 kΩ series resistors)						
ARINC input voltage						
one or zero	V_{DIN}	Differential voltage	6.5	10		V
null	V_{NIN}	" " "	-	-	2.5	V
common mode	V_{COM}	with respect to ground	-30.0	-	+30.0	V
ARINC input resistance						
RINA-R to RINB-R	R_{DIFF}	Supplies floating	-	200	-	kΩ
RINA-R or RINB-R to GND	R_{GND}	" "	-	140	-	kΩ
RINA-R or RINB-R to VCC	R_{VCC}	" "	-	100	-	kΩ
LOGIC INPUTS						
Input Voltage	V_{IH}	Input Voltage HI	70%			VDD
	V_{IL}	Input Votage LO			30%	VDD
Input Current (HI-8476 only)	I_{SINK}	V_{IN} = VDD, 25kΩ pull down	80	150	240	µA
(LLB7-0, LLC7-0, LLBEN, LLCEN pins)	I_{SOURCE}	V_{IN} = GND	-1			µA
Input Current	I_{SINK}	V_{IN} = VDD			1	µA
(All other inputs)	I_{SOURCE}	V_{IN} = GND	-1			µA
LOGIC OUTPUTS						
Output Voltage	V_{OH}	I_{OH} = -100µA	90%			VDD
	V_{OL}	I_{OL} = 100µA			10%	VDD
Output Current	I_{OL}	V_{OUT}= 0.4V	1.6			mA
	I_{OH}	V_{OUT} = VLOGIC - 0.4V			-1.0	mA
Tri-state Current (BIT1 - BIT32 only)	I_{OZH}	V_{IN} = VDD, 100kΩ pull down	20	40	60	µA
	I_{OZL}	V_{IN} = GND	-1			µA

D.C. ELECTRICAL CHARACTERISTICS (cont.)

VDD = 3.0 to 5.5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SUPPLY						
VDD Supply current	I_{DD5}	V_{DD} = 5.5V		5	8	mA
	I_{DD3}	V_{DD} = 3.6V		4	6	mA
CAPACITANCE						
Output Capacitance	C_O			15		pF
Output Capacitance	C_I			5		pF

AC ELECTRICAL CHARACTERISTICS

VDD = 3.0 to 5.5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
CLOCK						
CLKIN Frequency	f_{CLK}		0.99		1.01	MHZ
CLKIN Mark : Space Ratio	t_{CLKMS}		40		60	%
DATA RECEPTION						
Delay, ARINC 429 word received to BIT1-32 change	t_{UD}	SPEED = 1 (100kb/s ARINC 429)			10	µs
	t_{UD}	SPEED = 0 (12.5kb/s ARINC 429)			80	µs
Delay ARINC bit 1 to UPDATE low	t_{UL}	SPEED = 1 (100kb/s ARINC 429)			10	µs
	t_{UL}	SPEED = 0 (12.5kb/s ARINC 429)			80	µs
BIT1-32 change before UPDATE high	t_{BSU}	D = 1/CLKIN for High speed D = 8/(CLKIN) for Low speed	D - 50	D	D + 150	ns
SDAT valid before SCLK rising edge	t_{SVB}		150			ns
SDAT valid after SCLK rising edge	t_{SVA}		150			ns
RESET & SELF TEST						
Master Reset ($\overline{MR}$) Pulse width	t_{MR}		100			ns
TESTDIS to $\overline{MR}$ rising edge set-up time	t_{MTSU}		50			ns
TESTDIS after $\overline{MR}$ rising edge hold time	t_{MTH}		50			ns
Self-test execution time	t_{SFT}	SPEED = 1 (100kb/s ARINC 429)			400	µs
	t_{SFT}	SPEED = 0 (12.5kb/s ARINC 429)			3	ms
Delay MR rising to BIT default state	t_{DMR}				50	ns

TIMING DIAGRAMS

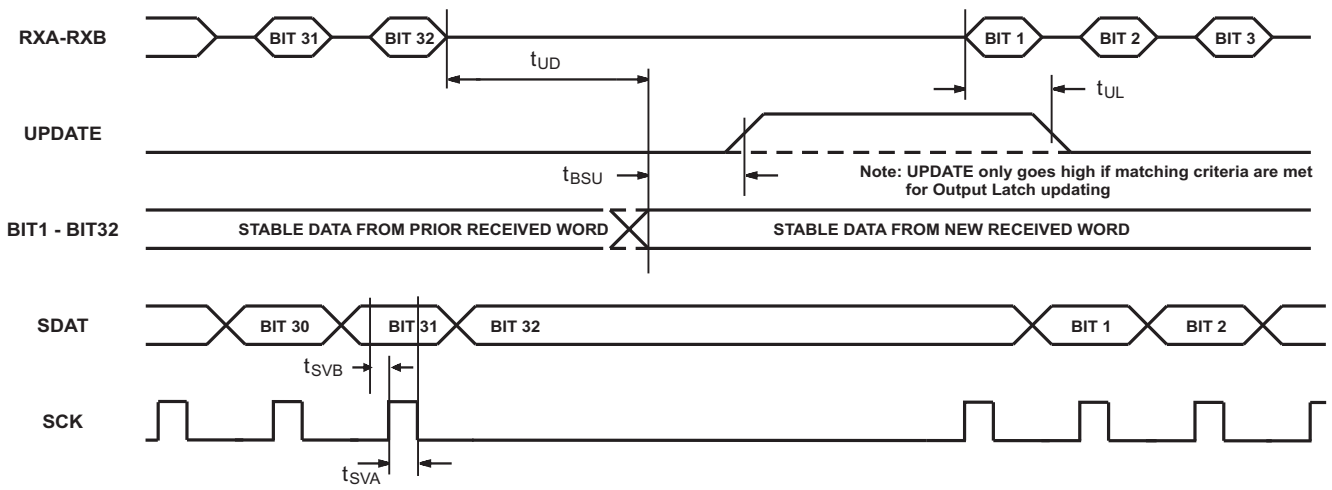


Figure 6. ARINC 429 Data reception timing

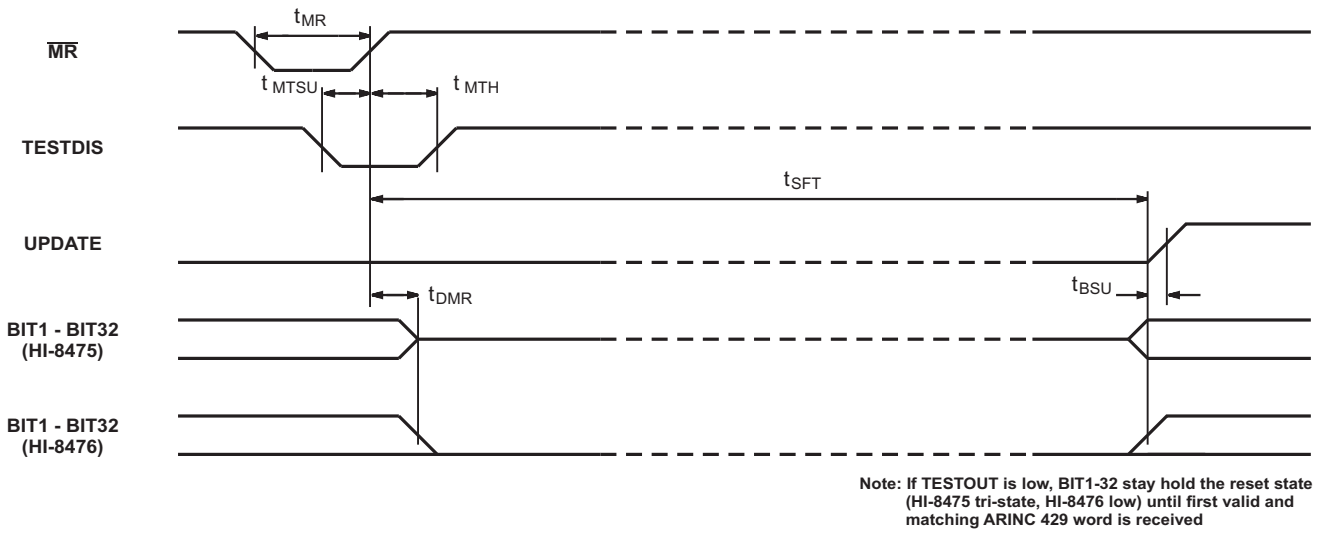


Figure 7. Reset and Self-Test timing

ORDERING INFORMATION

HI - 847xPQ x F

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION
8475PQ	64 PIN PLASTIC QUAD FLATPACK (PQFP)
8476PQ	128 PIN PLASTIC QUAD FLATPACK (PQFP)

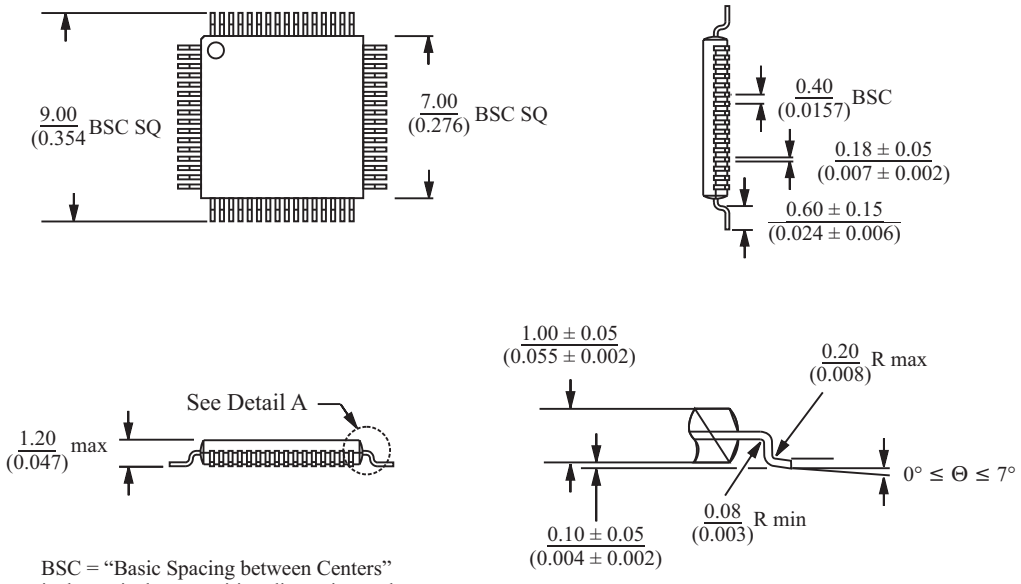
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8475	New	11/1/13	Initial Release
	A	11/20/14	Clarify that 13kOhm external resistors must be used on ARINC 429 receiver inputs for RTCA/DO-160G Level 3 lightning protection.

64 PIN PLASTIC THIN QUAD FLAT PACK (TQFP)

milimeters (inches)

Package Type: 64PQS

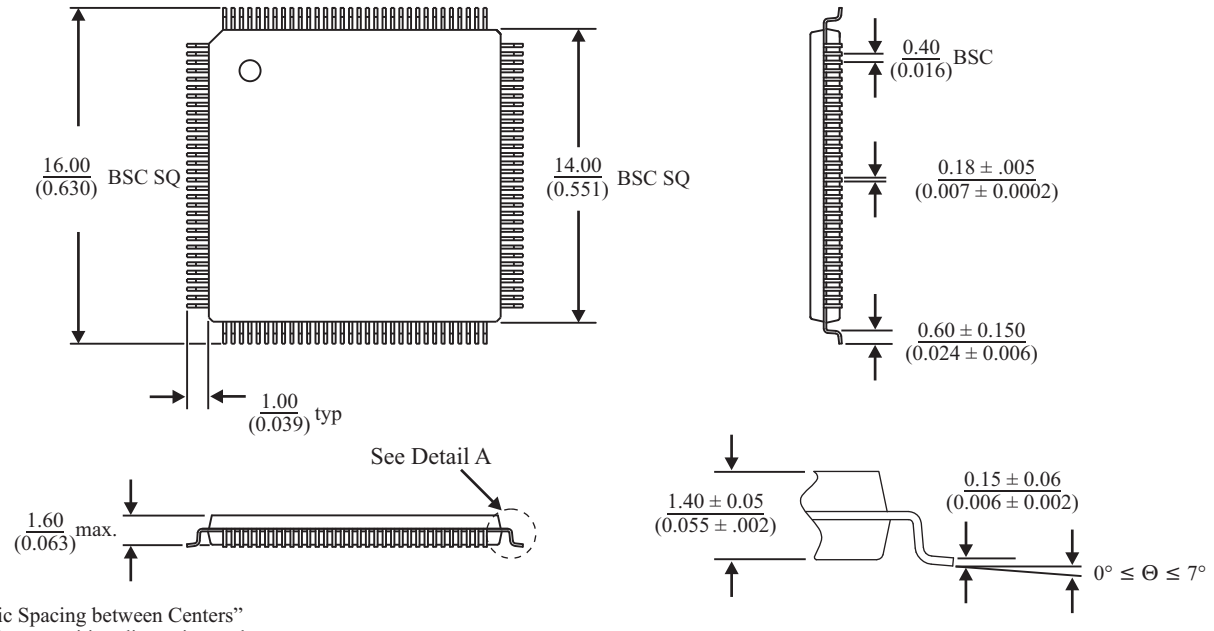


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

128-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 128PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)