HOLT INTEGRATED CIRCUITS

AN-6130-2

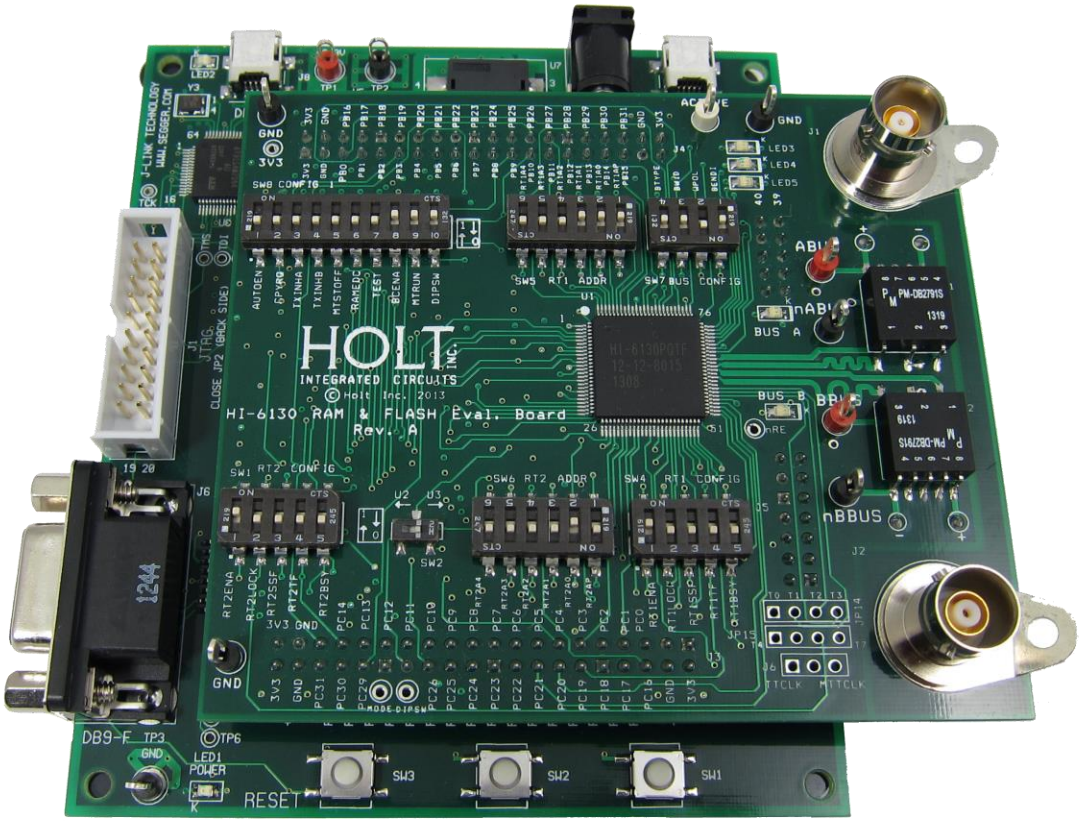
HI-6130 API Application Development Kit

December 12, 2018

Introduction

The Holt HI-6130-2 Application Development Kit (ADK) demonstrates the broad feature set of the HI-6130 Multi Terminal IC for MIL-STD-1553. The 2-board assembly and C project reference design provides a ready-to-run evaluation platform demonstrating concurrent operation for any combination of Bus Controller, Bus Monitor and one or two Remote Terminals. For convenience, this kit includes IAR Systems *Embedded Workbench® for ARM*, and a fully integrated debug interface for the ARM Cortex M3 microcontroller.

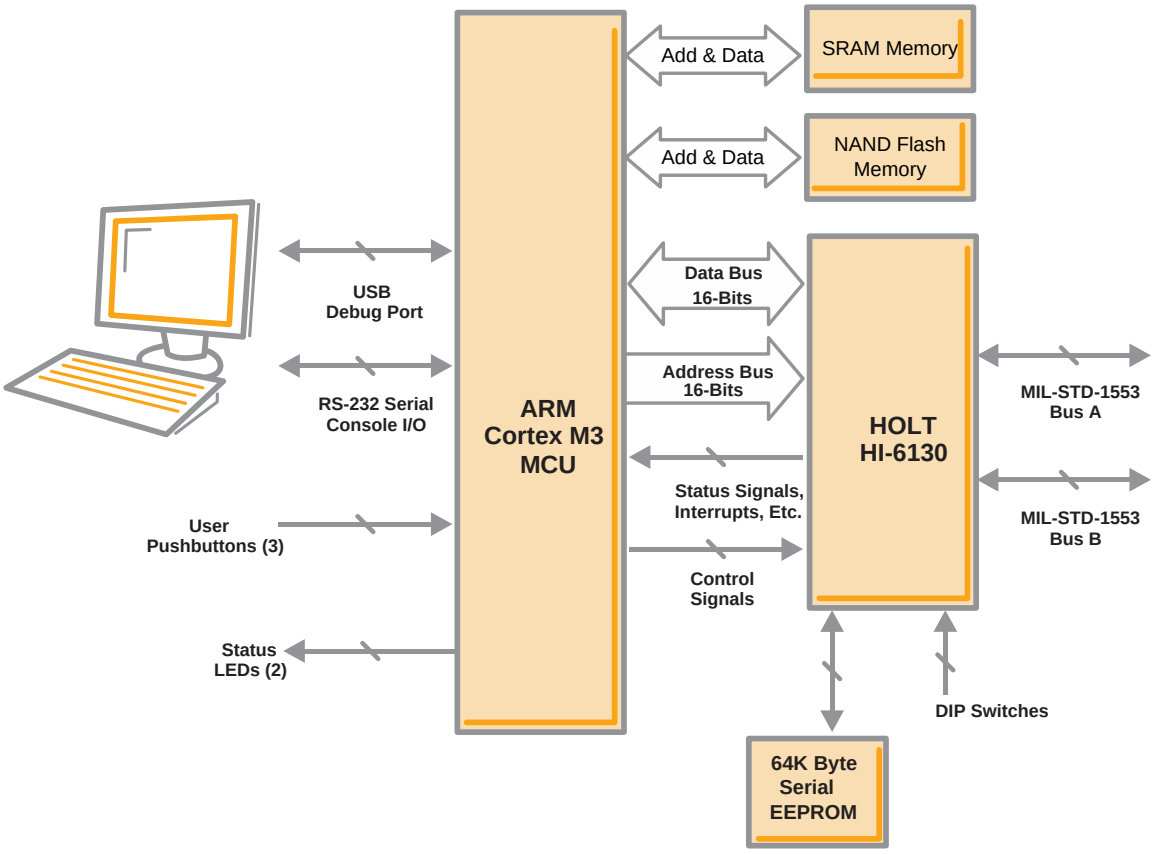
This guide describes how to set up and run the board. Additional support material and all required project software are found in the included Holt CD-ROM. A version of the demonstration software is already programmed into the microcontroller flash; the board is operational right out of the box without installing or running the provided software development tools.



Evaluation Kit Contents

- This User Guide.
- Holt HI-6130-2 Holt API Project Software and Documentation CD.
- Holt API high-level software library and users guide.
- Installation CD for IAR Systems *Embedded Workbench® for ARM*, version 7.1 or greater.
- Plug-in 5V DC power supply.
- USB debug interface cable.
- RS-232 serial cable, DB-9M to DB-9F for console I/O using a connected computer.
- The two board HI-6130-2 ADK is comprised of…
    - Upper HI-6130 board with dual transformer-coupled MIL-STD-1553 bus interfaces. Numerous DIP switches configure board operation. Compared to the standard HI-6130 ADK, host-accessible NAND Flash and SRAM memory are added to demonstrate application-level memory management by the host MCU. The NAND flash IC is currently not used.
    - Lower MCU board with ARM Cortex M3 16/32-bit microprocessor, debug interface and regulated 3.3VDC power supply.

Hardware Block Diagram



Hardware Design Overview

The end of this guide provides separate schematic diagrams and bills of material for the upper and lower circuit boards.

In contrast to the standard HI-6130 ADK, the HI-6130-2 ADK upper board has additional SRAM and NAND Flash (Flash is currently not used). This supports host memory management by the host when running high-level applications written in C. To fulfill application requirements, such programs may use Holt API function calls to move data between system resources (such as SRAM) and HI-6130 device memory. This kit's demo programs show how to use API function calls when initializing the system or when loading (or off-loading) HI-6130 registers or data buffers from (or to) system SRAM.

The detachable HI-6130-2 upper daughter board can be separated from the provided MCU board for connection to a user-supplied alternate microprocessor or FPGA board. The inter-board headers are located on 0.1" (2.54 mm) grid for compatibility with generic prototyping boards. All host interface signals go through the inter-board headers. Numerous HI-6130 configuration pins (and the Remote Terminal address setting pins) are controlled by DIP switches on the upper HI-6130 board; these signals are not available on the inter-board headers.

The lower ARM Cortex M3 board is based on the flash-programmable Atmel AT91SAM3U-EK microprocessor. A 16-bit parallel bus interface connects to the HI-6130. A UART-based serial port provides RS-232 console I/O (optional). An uncommitted USB 2.0 port is available for future expansion. Two pushbuttons are available for software interaction. A RESET pushbutton resets the ARM microprocessor, which in turn controls the HI-6130 Master Reset signal.

The ARM Cortex M3 board includes "J-Link On Board" debug interface, licensed from www.segger.com, providing out-of-box readiness without having to buy a costly JTAG debug cable. The kit includes a simple USB cable for connecting the board's debug interface to your computer. (For users already owning an ARM debug interface with ribbon-cable connector, an ARM-standard 2x10 debug connector provides debug connectivity. In this case, jumper JP2 on the bottom of the lower board should be soldered closed to disable "J-Link On Board".)

A Quick Demonstration

The Holt HI-6130-2 Application Development Kit is pre-programmed to concurrently operate as a Bus Controller, SMT Bus Monitor and two independent Remote Terminals (RT and RT2). Terminal addresses for the two RTs are preset using DIP switches, before applying power. The RT1 DIP switches should be set to RT address 3 (0-0-0-1-1-parity 1), RT2 should be set to RT address 1 (0-0-0-0-1-parity 0), to work with the demonstration program utilized by the preprogrammed Bus Controller message repertoire. The two 6-position DIP switches should already be set with these address values, plus odd parity. The user's guide, source code and software documentation sometimes refers RT1 as just RT.

1. Follow this quick demonstration of the demo board before installing IAR Systems *Embedded Workbench® for ARM* (EWARM) and the Holt demo project folders to ensure the board operates stand-alone. The demo program is already programmed into the flash memory in the Atmel CM3 processor so it can be demonstrated right out of the box. Install IAR EWARM and the Holt demo projects later, when instructed to do so.

2. The demonstration program uses the console (serial port to the PC) to provide a command menu and to display message traffic information. Use console I/O with a computer serial (COM) port and a "terminal emulation" program like *TeraTerm*. Most desktop computers have a COM port; many notebook computers do not have a COM port; these require a serial-to-USB adapter (not provided by the Holt ADK).

   Windows 7 is recommended. The installation instructions refer to *Windows* 7 directory names.

   Install the free open-source terminal emulation program, *TeraTerm 4.71*, by running the provided `teraterm-4.71.exe` installer program from the Holt CD. Accept the license agreement stating redistribution is permitted provided that copyright notice is retained. The notice can be displayed from the *TeraTerm* window by clicking **Help** then clicking **About TeraTerm**. Continuing to install…

   - Accept the default install destination and click **Next**.
   - At the Select Components screen, unselect all options except Additional Plugin = TTXResizeMenu and click **Next**.
   - Select the installed language, then click **Next**.
   - Accept the default Start Menu folder, then click **Next**.
   - Select any desired shortcuts, then click **Next**.
   - At the Ready to Install screen, click **Install**.

Run the *TeraTerm* program. At the **New Connection** screen, select **(x)Serial** and choose the selected COM port. Click **Setup** then **Serial Port** to open the serial port setup window. Choose these settings: Baud Rate: 115200, Data: 8 bits, Parity: none, Stop: 1 bit, Flow Control: none
Using the provided DB-9 serial cable, connect the MCU board to the computer serial (COM) port.

3. After configuring the Console port, connect the DB-9 serial cable to the PC.

4. Do not connect the included USB debugger cable between the DEBUG port on the lower (MCU) board and the PC until instructed to, later.

5. To observe bus activity, connect an oscilloscope to the red test points labeled BUS A and BUS B. The test point labeled ACTIVE is a convenient scope trigger signal that goes high at start of message and goes low at message completion.

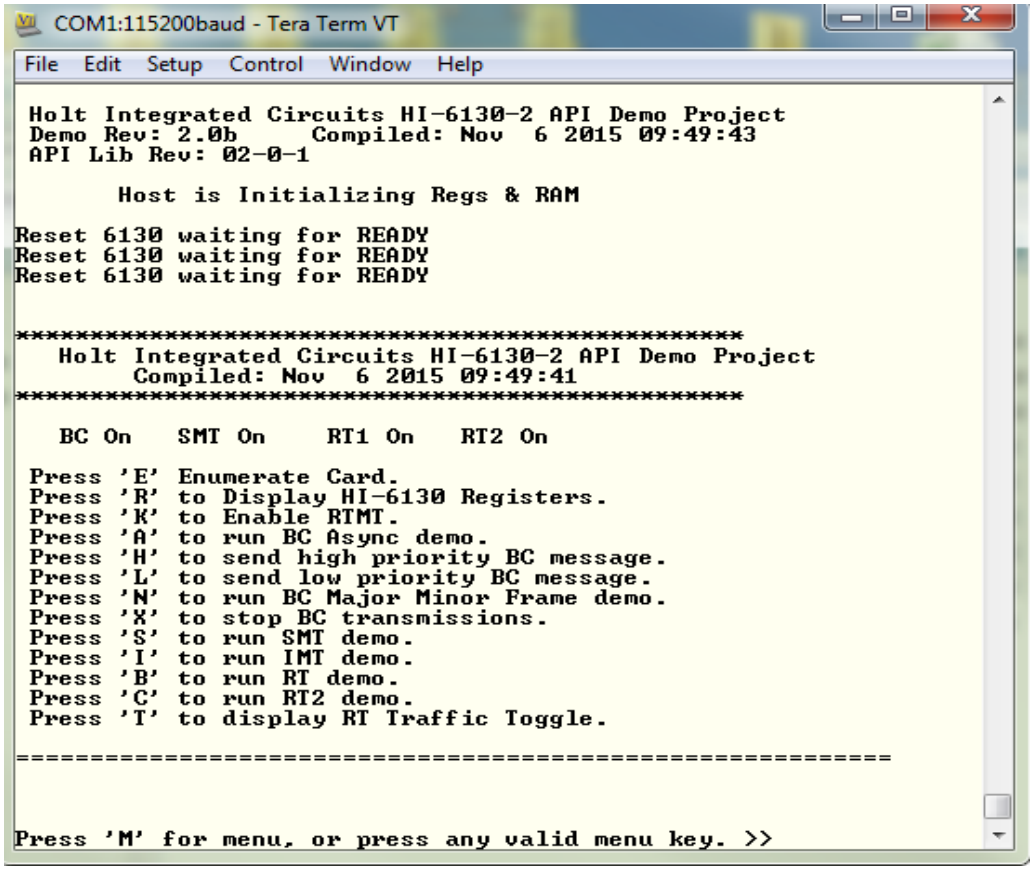
6. If not connected by cable to actual MIL-STD-1553 buses, provide resistive dummy loads for buses A and B by connecting a 75 Ω 1/2 Watt (or any value between 70-80 Ω) resistor across each pair of red and black Bus test points. (For this demonstration, half-Watt resistors are adequate because duty cycle is sufficiently low. When using the on-chip HI-6130 to generate BC messages directed to on-chip RTs, use external 75 Ω resistor loads. When using a bus coupler to connect to actual MIL-STD-1553 buses, do not use the 75 Ω dummy load resistors.

7. Set SW8 configuration DIP switches labeled AUTOEN and COPYREQ off (down position). These switches are not used by this version of the demo program so they can be repurposed by the user.

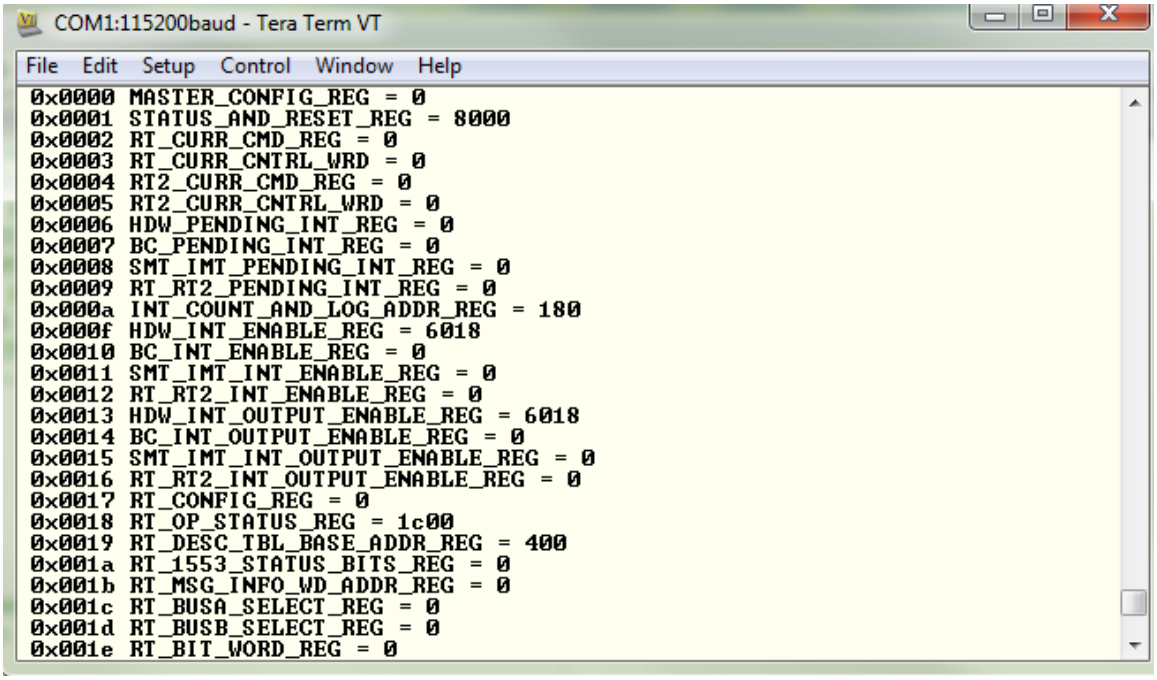
8. Plug-in the provided 5V DC power supply and connect the cable to the power input jack on the lower circuit board. If TeraTerm is running and configured correctly, the command menu below should appear in the console window.

9. This menu appears and three green LEDs will flash momentarily whenever the board power is applied, or when the RESET pushbutton is pressed. After verifying correct *TeraTerm* communication with the evaluation board, the terminal set up can be saved by clicking **Setup** then **Save Setup**.

The dates and times shown may appear differently from the screen shown.



Press 'R' or 'r' to display the HI-6130 system registers. Commands can be entered upper or lower case.



General structure of demo functions

The Holt API demonstration program is contained in module "demos.c". The API libraries are contained in the library file "Holt 613x API LIB.a" as executable object code. "Demos.c" contains the demo initialization API function calls supporting demonstrations executed from the console menu to initialize the BC, RT(s) and monitor terminals. Key presses are detected in "console.c" which is called from the main loop in "main.c" and executes demo functions in "demos.c".

Commands 'A' and 'N' transmit BC commands and can be viewed on an oscilloscope and optionally display the message traffic data on the console using the 'K' and 'T' command sequence. These demos demonstrate how Holt API's are used to generate BC Asynchronous messages, Major/Minor frames, low priority and high priority messages. View these messages with external MIL-STD-1553 test equipment or view them with an oscilloscope.

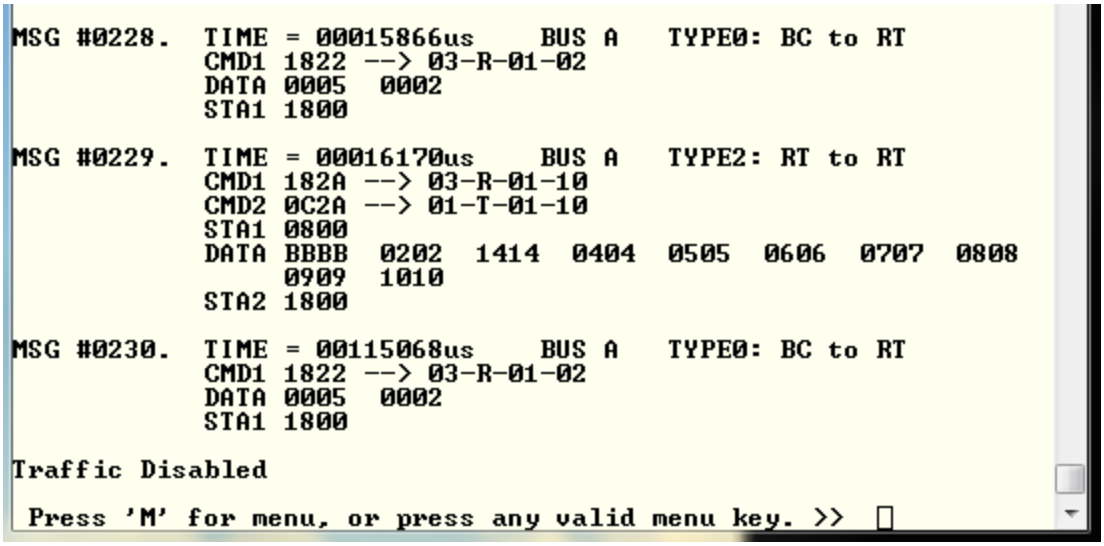
This exercise uses the internal BC to transmit messages, so message traffic data is displayed on the console. Since the internal BC, RTs and SMT share the same bus pins, the RT and SMT monitor terminals receive the BC messages. If an external BC is already connected to the bus jack though a bus coupler, it is okay to leave it connected, but disable any external BC transmissions that will conflict with the on-chip BC transmissions. Without an external BC connected, connect an external 75Ω 1/2 Watt resistor across the BUSA and nBUSA test points to terminate the bus. These are the red and black test points adjacent to the round 1553 Bus A jack.

Internal BC demo with RT Traffic on console

10. Press command 'B' and 'C' to enable both RTs.
11. Press command 'K' to enable the RTMT demo.
12. Press command 'T' (or spacebar) to display RT traffic on the console. Command 'T' toggles on and off alternately to enable or disable the RT traffic shown on the console. Using the 'T' command relies on prior execution of command 'K'.

13. Press command ‘A’ to start the BC transmitting messages.

    Messages will display rapidly on the screen, Press the space bar to stop the console output. The console should freeze and look similar to the screen below. Press space bar again to restart the console output. Using the space bar does not stop BC transmission or prevent RT or MT message reception; it only stops console output.

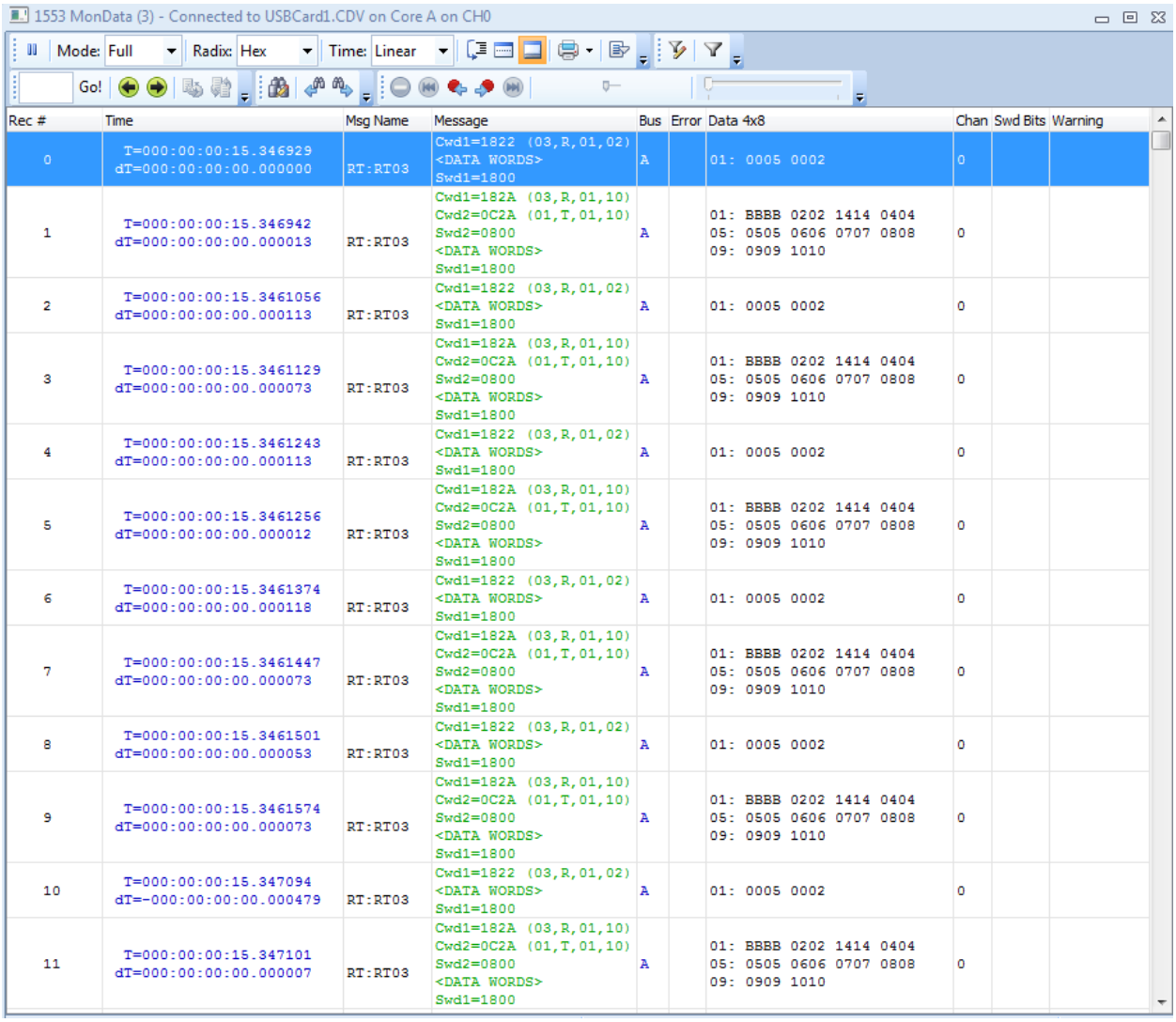


    The following screen shot (on next page) shows a partial listing of messages captured while running the BC Async demo. The transmissions shown on the next page were captured using a Ballard USB 1553 monitor.

    The Bus A green LED flashes rapidly (but appears continuously lit) with this demo.

14. Repeating this sequence without RT2 ‘C’ enabled causes the Bus B green LED to flash because some BC messages are configured to retry on Bus B when there is no RT response from Bus A. Press RESET, Press ‘B’, Press ‘K’ and Press ‘T’ or (spacebar) then Press ‘A’. Both Bus LEDs should flash.

15. From a RESET, if the BC is started before enabling the ‘K’ and ‘T’ sequence to display message traffic, the first message may contain an error. This is normal; this occurs because the RT and MT are enabled midstream of a message in progress.



Rec #	Time	Msg Name	Message	Bus	Error	Data 4x8	Chan	Swd Bits	Warning
0	T=000:00:00:15.346929 dT=000:00:00:00.000000	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
1	T=000:00:00:15.346942 dT=000:00:00:00.000013	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		
2	T=000:00:00:15.3461056 dT=000:00:00:00.000113	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
3	T=000:00:00:15.3461129 dT=000:00:00:00.000073	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		
4	T=000:00:00:15.3461243 dT=000:00:00:00.000113	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
5	T=000:00:00:15.3461256 dT=000:00:00:00.000012	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		
6	T=000:00:00:15.3461374 dT=000:00:00:00.000118	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
7	T=000:00:00:15.3461447 dT=000:00:00:00.000073	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		
8	T=000:00:00:15.3461501 dT=000:00:00:00.000053	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
9	T=000:00:00:15.3461574 dT=000:00:00:00.000073	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		
10	T=000:00:00:15.347094 dT=-000:00:00:00.000479	RT:RT03	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: 0005 0002	0		
11	T=000:00:00:15.347101 dT=000:00:00:00.000007	RT:RT03	Cwd1=182A (03,R,01,10) Cwd2=0C2A (01,T,01,10) Swd2=0800 <DATA WORDS> Swd1=1800	A		01: BBBB 0202 1414 0404 05: 0505 0606 0707 0808 09: 0909 1010	0		

16. BC low priority message insertion.

Command 'L' inserts a low priority message into the BC transmissions. First, enable both RTs by pressing 'B' and 'C' then Press 'A' to enable the BC transmissions. Press 'L' to transmit three extra messages on Bus B. Bus B is used to make it easier to see on the scope and the Bus B LED should flash. If the RTs were not enabled, retry messages would appear on bus B making it more difficult to see the three inserted messages. This will only work once after a power up or RESET.

Rec #	Time	Message	Bus	Error	Data 4x8	Chan	Swd Bits	Warning
0	T=000:00:0... dT=000:00:0...	Cwd1=0822 (01,R,01,02) <DATA WORDS> Swd1=0800	B		01: DEAD BEEF	1		
1	T=000:00:0... dT=000:00:0...	Cwd1=0C2F (01,T,01,15) <DATA WORDS> Swd1=0800	B		01: BBBB 0202 1414 ... 05: 0505 0606 0707 ... 09: 0909 1010 1111 ... 13: 1313 1414 1515	1		
2	T=000:00:0... dT=000:00:0...	Cwd1=0825 (01,R,01,05) <DATA WORDS> Swd1=0800	B		01: CAFE CODE 0303 ... 05: 0505	1		

17. BC High priority message insertion.

Follow the same steps as the previous BC low priority message example but this time Press 'H' to insert a single high priority message. This command is repeatable and the Bus B LED will flash with each command.

T=000:00:0... dT=000:00:0...	Cwd1=0822 (01,R,01,02) <DATA WORDS> Swd1=0800	B		01: DEAD BEEF	1	

18. **Command 'E'** Enumerate Card is reserved for future use.

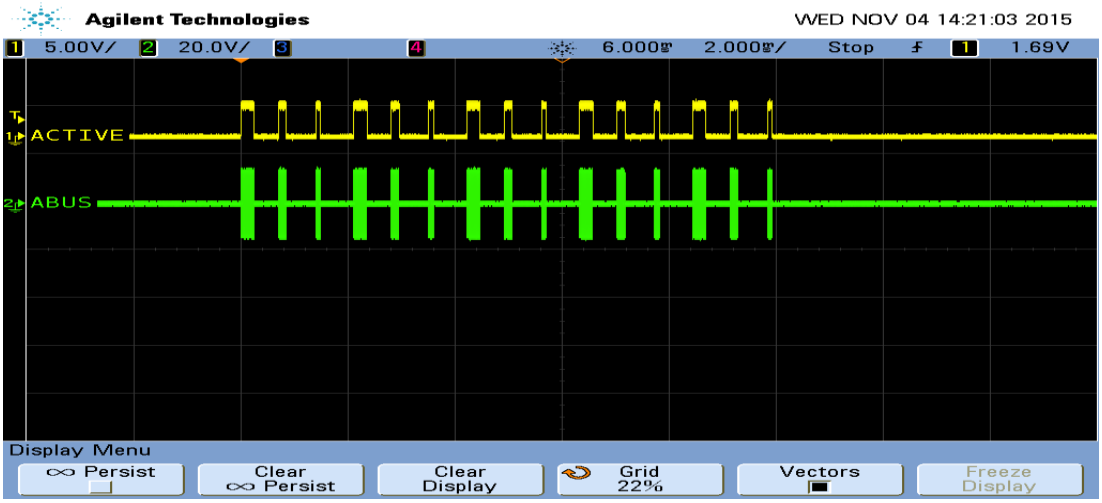
19. The 'N' command transmits fifteen commands to RT address 3. Press 'B' to enable the RT.

The RT naming might be confusing and needs further explanation: There are two RT terminals in the HI-6130 device. The two RT terminals have their own RT address DIP switches on the board to allow setting the RT address for each.

The first RT (referred to as RT or RT1) is set for RT address 3.

The second RT (RT2) is set for RT address 1.

Press 'N' to execute the BC transmissions (15 messages are transmitted) which will appear on the bus as shown below. To optionally see the message traffic on the console, enable the RT message traffic by pressing 'T' if it hasn't already been enabled.



Command ‘N’ (15 message) Traffic capture using a Ballard USB 1553 monitor.

Rec #	Time	Message	Bus	Error	Data 4x8	Chan	Swd Bits	Warning
0	T=000:00:00:00.1583950 dT=000:00:00:00.000000	Cwd1=1C2A (03,T,01,10) <DATA WORDS> Swd1=1800	A		01: 1000 1001 1002 1003 05: 1004 1005 1006 1007 09: 1008 1009	0		
1	T=000:00:00:00.15831208 dT=000:00:00:00.000258	Cwd1=1825 (03,R,01,05) <DATA WORDS> Swd1=1800	A		01: AAAA 0202 0303 0404 05: 0505	0		
2	T=000:00:00:00.15831466 dT=000:00:00:00.000257	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: BBBB 0202	0		
3	T=000:00:00:00.1584128 dT=-000:00:00:00.000337	Cwd1=1C2A (03,T,01,10) <DATA WORDS> Swd1=1800	A		01: 1000 1001 1002 1003 05: 1004 1005 1006 1007 09: 1008 1009	0		
4	T=000:00:00:00.1584446 dT=000:00:00:00.000318	Cwd1=1825 (03,R,01,05) <DATA WORDS> Swd1=1800	A		01: AAAA 0202 0303 0404 05: 0505	0		
5	T=000:00:00:00.1584704 dT=000:00:00:00.000258	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: BBBB 0202	0		
6	T=000:00:00:00.1584967 dT=000:00:00:00.000262	Cwd1=1C2A (03,T,01,10) <DATA WORDS> Swd1=1800	A		01: 1000 1001 1002 1003 05: 1004 1005 1006 1007 09: 1008 1009	0		
7	T=000:00:00:00.15841224 dT=000:00:00:00.000256	Cwd1=1825 (03,R,01,05) <DATA WORDS> Swd1=1800	A		01: AAAA 0202 0303 0404 05: 0505	0		
8	T=000:00:00:00.15841542 dT=000:00:00:00.000318	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: BBBB 0202	0		
9	T=000:00:00:00.1585205 dT=-000:00:00:00.000337	Cwd1=1C2A (03,T,01,10) <DATA WORDS> Swd1=1800	A		01: 1000 1001 1002 1003 05: 1004 1005 1006 1007 09: 1008 1009	0		
10	T=000:00:00:00.1585463 dT=000:00:00:00.000258	Cwd1=1825 (03,R,01,05) <DATA WORDS> Swd1=1800	A		01: AAAA 0202 0303 0404 05: 0505	0		
11	T=000:00:00:00.1585721 dT=000:00:00:00.000257	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: BBBB 0202	0		
12	T=000:00:00:00.15851043 dT=000:00:00:00.000321	Cwd1=1C2A (03,T,01,10) <DATA WORDS> Swd1=1800	A		01: 1000 1001 1002 1003 05: 1004 1005 1006 1007 09: 1008 1009	0		
13	T=000:00:00:00.15851301 dT=000:00:00:00.000258	Cwd1=1825 (03,R,01,05) <DATA WORDS> Swd1=1800	A		01: AAAA 0202 0303 0404 05: 0505	0		
14	T=000:00:00:00.15851565 dT=000:00:00:00.000264	Cwd1=1822 (03,R,01,02) <DATA WORDS> Swd1=1800	A		01: BBBB 0202	0		

When a BC message is transmitted to a RT that is not enabled, “RT no response” (NORES) error is indicated.

```
MSG #0170.  TIME = 00086918us    BUS A   TYPE2: RT to RT
            CMD1 182A --> 03-R-01-10
            CMD2 0C2A --> 01-T-01-10
 ERROR: NORES
```

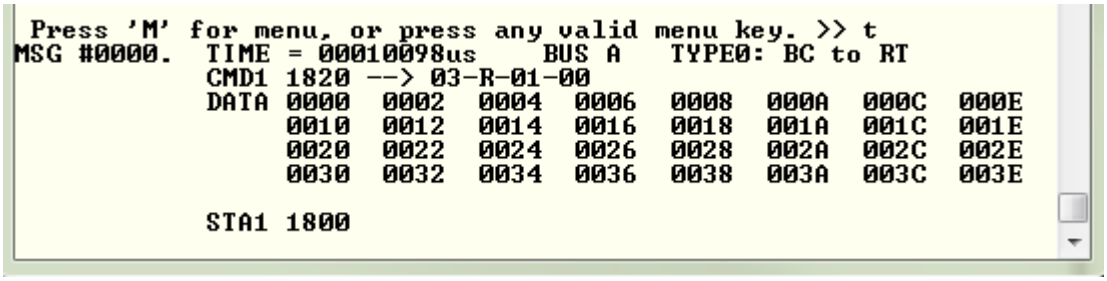
Commands ‘S’ and ‘I’

These demo commands initialize the SMT or IMT monitor features in the HI-6130 and return to the main menu, they do not display any information on the console. The SMT is also initialized and used in the ‘T’ RT Traffic command.

Using an external BC (such as Ballard tester) to transmit messages to the demo board.

When using a BC connected using a properly-terminated external bus to transmit commands to the RT or SMT, remove external 75 Ω resistors (if present) and connect the BC test equipment to the demo board circular tri-axial bus jacks using MIL-STD-1553 cables and bus couplers. If a bus coupler is not readily available, connect BC tester directly to the demo board tri-axial jack, but in this case use the 75 Ω termination resistor.

Press the RESET button and then Press 'B' or 'C" to enable both RT's then Press 'K' and 'T' to activate the RT traffic on the console. Compose a BC to RT message with SA=1 and 32 data words similar to the message shown below. The console should show the message transmitted by the BC, after the transaction.



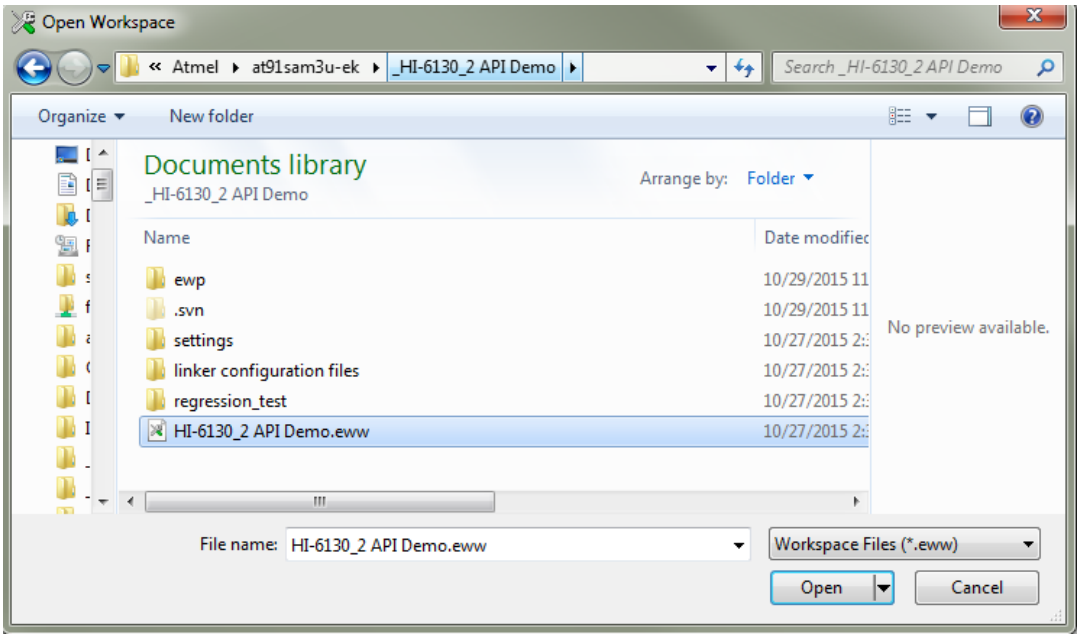
When transmitting repeating messages at a high rate typical of MIL-STD 1553, the RT Traffic shown on the console may not keep pace due to limitations of the console 115,200 baud rate. Depending on the message content and repetition rate, some messages may not show on the console. All messages are transacted properly and captured by enabled RT and MT, some messages simply will not be shown on the console.

Holt API function calls are fully described in the Holt API User's Guide HI-6130-API_xx.pdf included in the ADK CD-ROM.

Getting Started with the Holt API demo software project and Installing IAR Systems *Embedded Workbench for ARM* Compiler

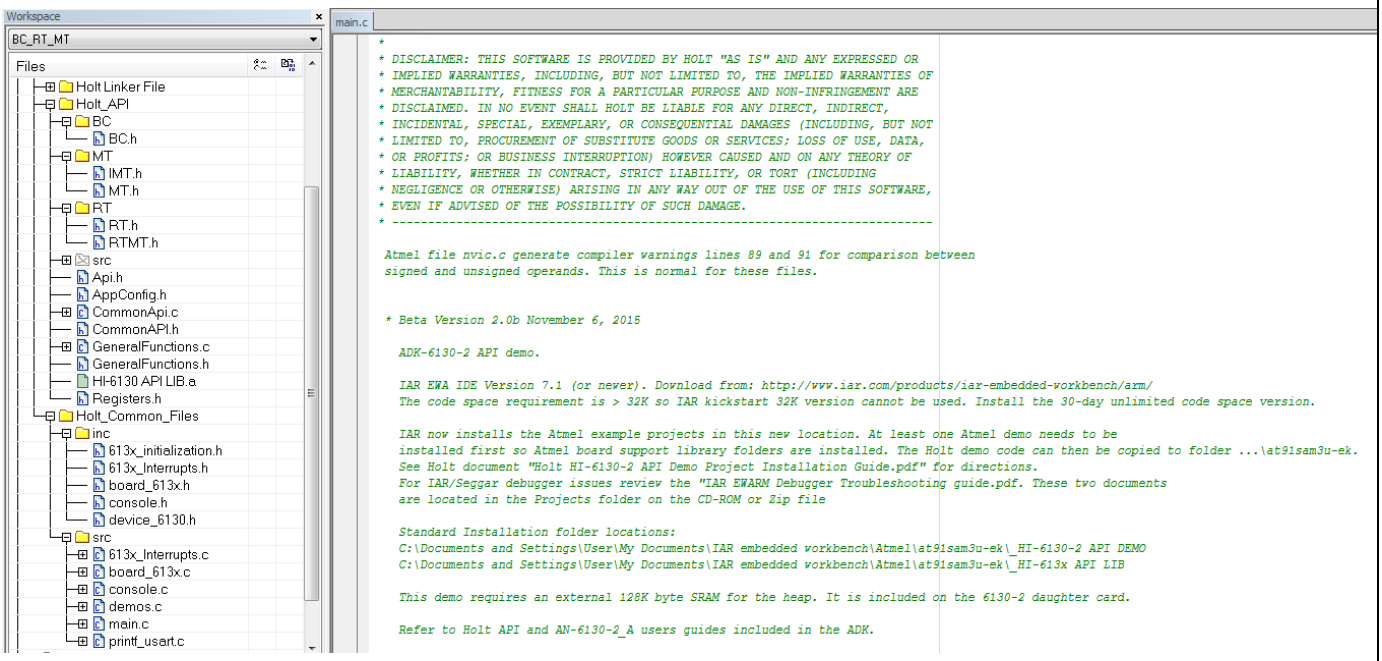
1. Installed IAR Systems *Embedded Workbench for ARM* (*EWARM*) compiler is required BEFORE adding the Holt demo projects so all Atmel board library files and the demo project folder are created in the proper location. Follow *the "Holt HI-6130-2 API Demo Project Installation Guide"* found in the Project folder on the Holt CD-ROM. Before proceeding to the next steps IAR must be installed and the two Holt project folders must be in the proper folder locations, according to that guide. **Instructions beyond this point assume you have completed the above installation tasks.**

2. Launch IAR *Embedded Workbench* from the Windows Start menu. A blank screen should appear. Open the Holt HI-6130-2 API Demo Project from the IAR File pull-down menu, click on File/Open/Workspace and navigate to the project folder location and select "HI-6130_2 API Demo.eww" and click the Open button.

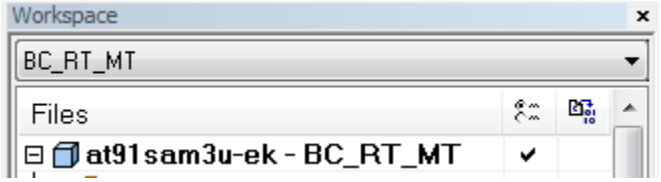


3. A Workspace window should appear on the left side as shown below. If the Workspace directory pane is missing, select “Workspace” from the View pull-down menu. Make any window adjustments or open any of the folder groups to view included files to suit your preferences.

4. Double click the “main.c” file, it should appear in the text editor pane, similar to this…



There are pre-configured 1553 terminal selections (IAR project configurations) chosen by a pull-down menu above the Files directory tree; the default is BC_RT_MT shown at the top. Some configurations exclude file groups and files from the compiler/linker build. For example if the “BC Only” configuration is selected, folders and files not needed are dimmed indicating the project will not use those files on the next build. Modifying or creating new configurations is easy from the Project pull down menu. See IAR IDE project documentation from the Help menu for more information on project configurations. Holt provides C code files for the 1553 API Runtime Library to customers who have signed a non-disclosure agreement (NDA). These files are not included in the standard ADK. Attempting to select the BC_RT_MT_FULL configuration and build it will cause multiple compiler/linker errors without the API C files. The API C source files are not required to use the API since those are prebuilt into an executable-code Library file “HI-6130 API LIB.a” used for all the other configurations. The default is shown below.



5. Debug requires an interface between the computer running IAR *Embedded Workbench®* and the HI-6130-2 Application Development Kit. Connect the small end of the provided USB cable to the HI-6130-2 evaluation board USB connector marked DEBUG. Connect the other end of the USB cable to a free computer USB port. The IAR C-SPY Debugger for ARM includes drivers for numerous target system interfaces, including built in "J-link On Board". Before the debug cable is plugged in, Debugger LED2 should flash repeatedly until the cable is connected to the PC.

   The first time the evaluation board USB cable is connected to the computer, the *Windows* "Found New Hardware" message should appear for the J-Link device. After several seconds, Windows should load the appropriate driver and advise, "Your hardware is ready for use". If Windows fails to find the J-Link driver, direct it to look in the Drivers directory the IAR *Embedded Workbench®* installation CD.

   If difficulties arise when initiating a debug session at step 11, click **Project** then **Options**. In the window that opens, under **Category** = **Debugger** highlight **J-Link/J-Trace**. Click the tab labeled **Connection**, then verify Communications = USB and Interface = SWD.

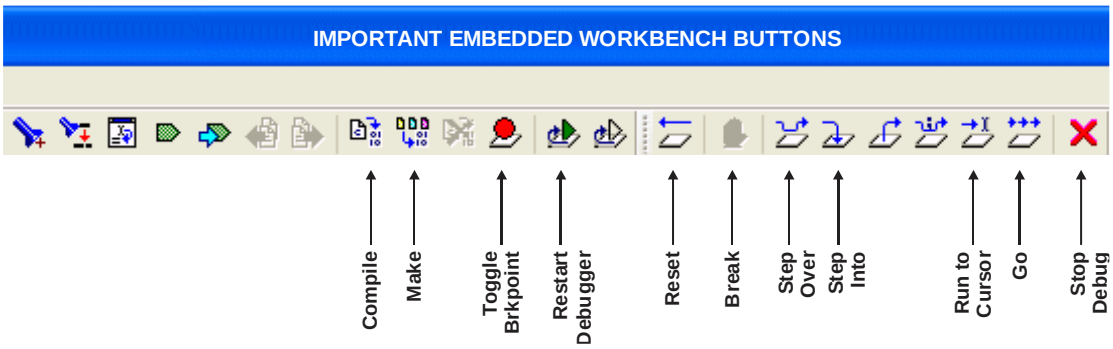
6. Optionally turn off the nuisance compiler message that occurs when a variable's most significant bit toggles. Some users prefer to see all warnings so in this case nothing is required. Some of the Atmel board files produces these warnings, the message looks like this:

   `Remark[Pe068]: integer conversion resulted in a change of sign`
   To optionally disable this diagnostic message, click **Project** then click **Options**
   Category = C/C++ Compiler
   Tab = Diagnostics
   `Suppress these diagnostics:` add "Pe068" to list

7. The default configuration BC_RT_MT enables the primary modes BC, MT, RT and RT2. This is the default configuration programmed into the demo board. This enables and demonstrates the Bus Controller, RT (RT1) and RT2 Remote Terminals and a Monitor. These configurations are all flash based projects. RAM based projects are not supported due to the limited amount of RAM on the MCU. By design the ARM Cortex-M3 runs slower in RAM than in Flash so there is little need for a RAM based project.

8. Compile the project by clicking the **Make** button. See following illustration. If the Build messages bottom pane in IAR *Embedded Workbench®* indicates no errors or warnings, you can continue. If errors occurred, correct them and recompile the program. Sometimes a "clean" build should be performed from the Project pull down window if strange compiler or linker issues occur.

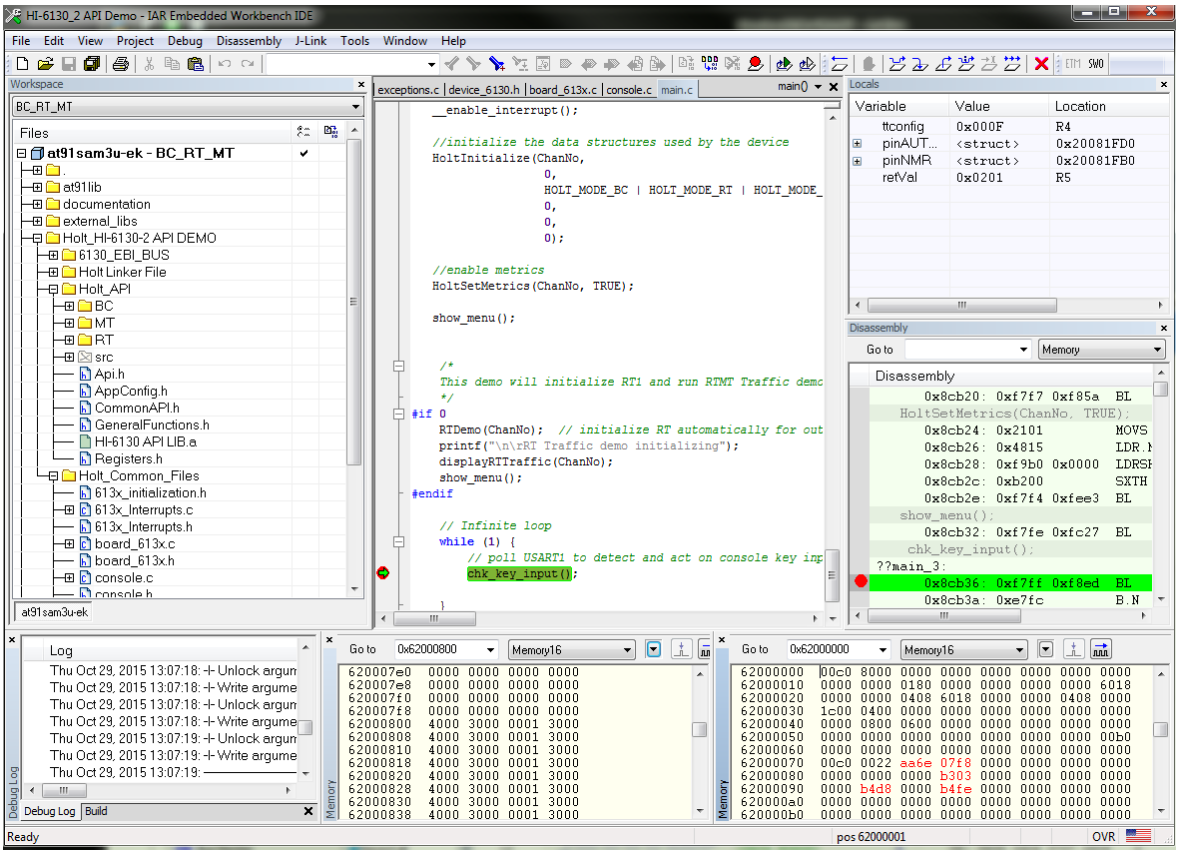
9. Initiate a debug session by clicking the **Restart Debugger** button. This downloads the compiled program into the MCU and readies the board for program execution. Click **Go** to start execution. Click **Break** (normally displayed during execution as a red upheld hand) to stop execution.



When execution starts the program menu will be displayed on the console and the green LED3, Bus A and Bus B LEDs will flash.

10. To observe bus activity, connect an oscilloscope to the red BUS A and red BUS B test points. The test point labeled ACTIVE is a convenient scope trigger signal.

11. It's possible to view multiple debugger windows including several memory windows. This allows viewing the system register space and control block areas of the HI-6130 to make debugging code easier. A breakpoint was set and executed below.


HI-6130_2 API Demo - IAR Embedded Workbench IDE
File Edit View Project Debug Disassembly J-Link Tools Window Help
Workspace
BC_RT_MT
Files
at91sam3u-ek - BC_RT_MT
at91lib
documentation
external_libs
Holt_HI-6130-2 API DEMO
6130_EBI_BUS
Holt Linker File
Holt_API
BC
MT
RT
src
Api.h
AppConfig.h
CommonAPI.h
GeneralFunctions.h
HI-6130 API LIB.a
Registers.h
Holt_Common_Files
613x_initialization.h
613x_Interrupts.c
613x_Interrupts.h
board_613x.c
board_613x.h
console.c
console.h
at91sam3u-ek
exceptions.c | device_6130.h | board_613x.c | console.c | main.c
main()
__enable_interrupt();
//initialize the data structures used by the device
HoltInitialize(ChanNo,
0,
HOLT_MODE_BC | HOLT_MODE_RT | HOLT_MODE_
0,
0,
0);
//enable metrics
HoltSetMetrics(ChanNo, TRUE);
show_menu();
/*
This demo will initialize RT1 and run RTMT Traffic demo
*/
#if 0
RTDemo(ChanNo); // initialize RT automatically for out
printf("\n\rRT Traffic demo initializing");
displayRTTraffic(ChanNo);
show_menu();
#endif
// Infinite loop
while (1) {
// poll USART1 to detect and act on console key inp
chk_key_input();
}
Locals
Variable Value Location
ttconfig 0x000F R4
pinAUT... <struct> 0x20081FD0
pinNMR <struct> 0x20081FB0
retVal 0x0201 R5
Disassembly
Go to
Memory
Disassembly
0x8cb20: 0xf7f7 0xf85a BL
HoltSetMetrics(ChanNo, TRUE);
0x8cb24: 0x2101 MOVS
0x8cb26: 0x4815 LDR.N
0x8cb28: 0xf9b0 0x0000 LDRSH
0x8cb2c: 0xb200 SXTH
0x8cb2e: 0xf7f4 0xfee3 BL
show_menu();
0x8cb32: 0xf7fe 0xfc27 BL
chk_key_input();
??main_3:
0x8cb36: 0xf7ff 0xf8ed BL
0x8cb3a: 0xe7fc B.N
Log
Thu Oct 29, 2015 13:07:18: -I- Unlock argun
Thu Oct 29, 2015 13:07:18: -I- Write argume
Thu Oct 29, 2015 13:07:18: -I- Unlock argun
Thu Oct 29, 2015 13:07:18: -I- Write argume
Thu Oct 29, 2015 13:07:19: -I- Unlock argun
Thu Oct 29, 2015 13:07:19: -I- Write argume
Thu Oct 29, 2015 13:07:19:
Debug Log
Build
Go to 0x62000800
Memory16
620007e0 0000 0000 0000 0000
620007e8 0000 0000 0000 0000
620007f0 0000 0000 0000 0000
620007f8 0000 0000 0000 0000
62000800 4000 3000 0001 3000
62000808 4000 3000 0001 3000
62000810 4000 3000 0001 3000
62000818 4000 3000 0001 3000
62000820 4000 3000 0001 3000
62000828 4000 3000 0001 3000
62000830 4000 3000 0001 3000
62000838 4000 3000 0001 3000
Go to 0x62000000
Memory16
62000000 00c0 8000 0000 0000 0000 0000 0000 0000
62000010 0000 0000 0180 0000 0000 0000 0000 6018
62000020 0000 0000 0408 6018 0000 0000 0408 0000
62000030 1c00 0400 0000 0000 0000 0000 0000 0000
62000040 0000 0800 0600 0000 0000 0000 0000 0000
62000050 0000 0000 0000 0000 0000 0000 0000 00b0
62000060 0000 0000 0000 0000 0000 0000 0000 0000
62000070 00c0 0022 aa6e 07f8 0000 0000 0000 0000
62000080 0000 0000 0000 b303 0000 0000 0000 0000
62000090 0000 b4d8 0000 b4fe 0000 0000 0000 0000
620000a0 0000 0000 0000 0000 0000 0000 0000 0000
620000b0 0000 0000 0000 0000 0000 0000 0000 0000
Memory
Ready
pos 62000001
OVR

Key Project Files with Selected Descriptions

HEADER FILES WITHOUT CORRESPONDING C FILES

HI-613x API LIB.a

Holt API library. Holt terminal demos use the Holt libraries to initialize and run the state machines. See the Holt API users guide for more information on the API's.

613x_initialization.h

Definitions for important configuration settings

device_6130.h

ARM MCU external bus interface definitions and structures for register addressing the HI- 6130.

C FILES WITH CORRESPONDING HEADER FILES

main.c

The primary program entry portal, `main()` demonstrates the initialization sequence and enters an endless loop waiting for console commands entered from the PC keyboard using the terminal program. When a BC, RT, SMT or IMT demo is selected on the console menu, corresponding demo functions execute in demos.c.

board_6130.c

This function initializes ARM MCU external bus interface for the HI-6130 and the 128K external SRAM.

console.c

This function looks for console key presses and executes corresponding demo commands.

For Holt API file descriptions see the API users guide.

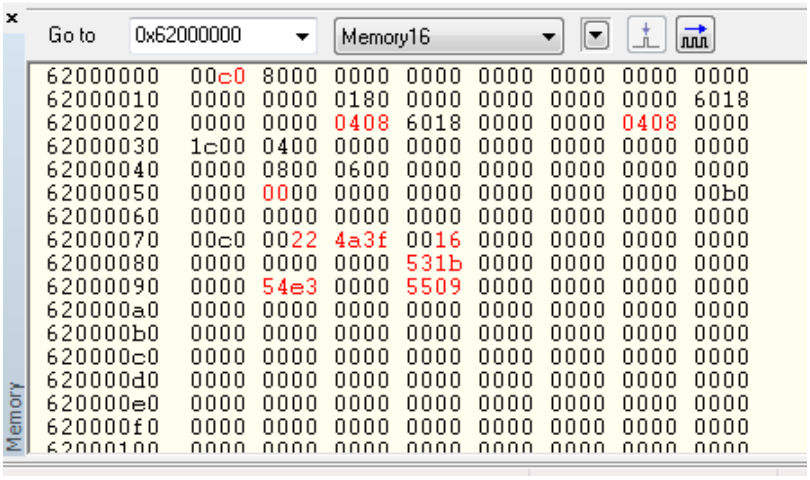
Application Development Kit Notes

The HI-6130 data sheet is included on the kit CD-ROM and the latest revision can be found at www.holtic.com. Primary project configuration settings are found in the header file **`613x_initialization.h`.**

The HI-6130 was designed for compatibility with microcontrollers having an external bus interface. RAM and register locations appear in the memory address space of the ARM Cortex M3 microprocessor on the MCU board. The utilized MCU chip select output (connected to the HI-6130 chip enable input pin) accesses a memory region starting at MCU bus address 0x62000000. Byte addressing is used. RAM and register operations transact 16-bit values, so all access addresses are even. To use byte addressing, HI-6130 RAM or register addresses are doubled and then added to the MCU chip select base address. Therefore, HI-6130 Register 0 is accessed at MCU bus address 0x62000000. Register 1 is accessed at bus address 0x62000002, and Register 5 is accessed at address 0x6200000A. An external 128K is required for the API demos and is located at starting address 0x6000-0000 to 0x6001FFFF. In the Holt linker file this space is assigned only for the heap for API buffers support.

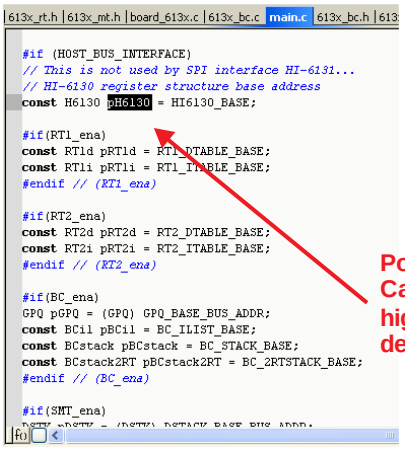
The evaluation board program provides comprehensive bus addressing examples for the fixed-address and relocatable RAM structures used by each of the MIL-STD-1553 terminal modes: BC, RT or monitor.

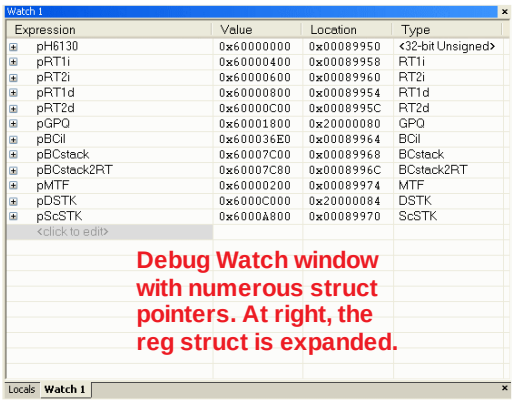
When using the Debugger, a Memory window may be helpful for observing register or RAM values, updated each time program execution stops. Be mindful that each displayed location is rescanned when execution stops. Some register or RAM structure bits automatically reset after read occurs. This includes bits in the Pending Interrupt registers, and DBAC Data Block Accessed bits for RT Descriptor Table Control Words in RAM. For these, the Memory Watch window reflects the value in effect when execution stopped.

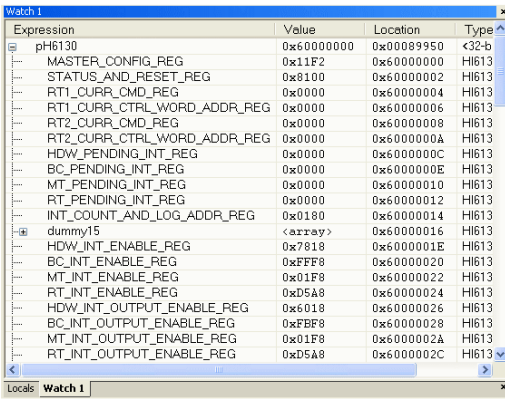


When using the Debugger, a Watch window may be helpful for observing values contained in the various defined RAM structures for enabled MIL-STD-1553 modes, updated each time program execution stops. When debugging, IAR Embedded Workbench® allows up to 4 Watch windows, so separate Watch tabs can be set up for BC, RT1, RT2, etc. For each structure of interest, double-click the

struct pointer name to highlight it, then drag and drop the highlighted pointer name into an open Watch window, where it can be examined. Be mindful that some RAM structure bits automatically reset after read occurs. This includes the DBAC Data Block Accessed bits for RT Descriptor Table Control Words. For these, the Memory Watch window reflects the value in effect when execution stopped.



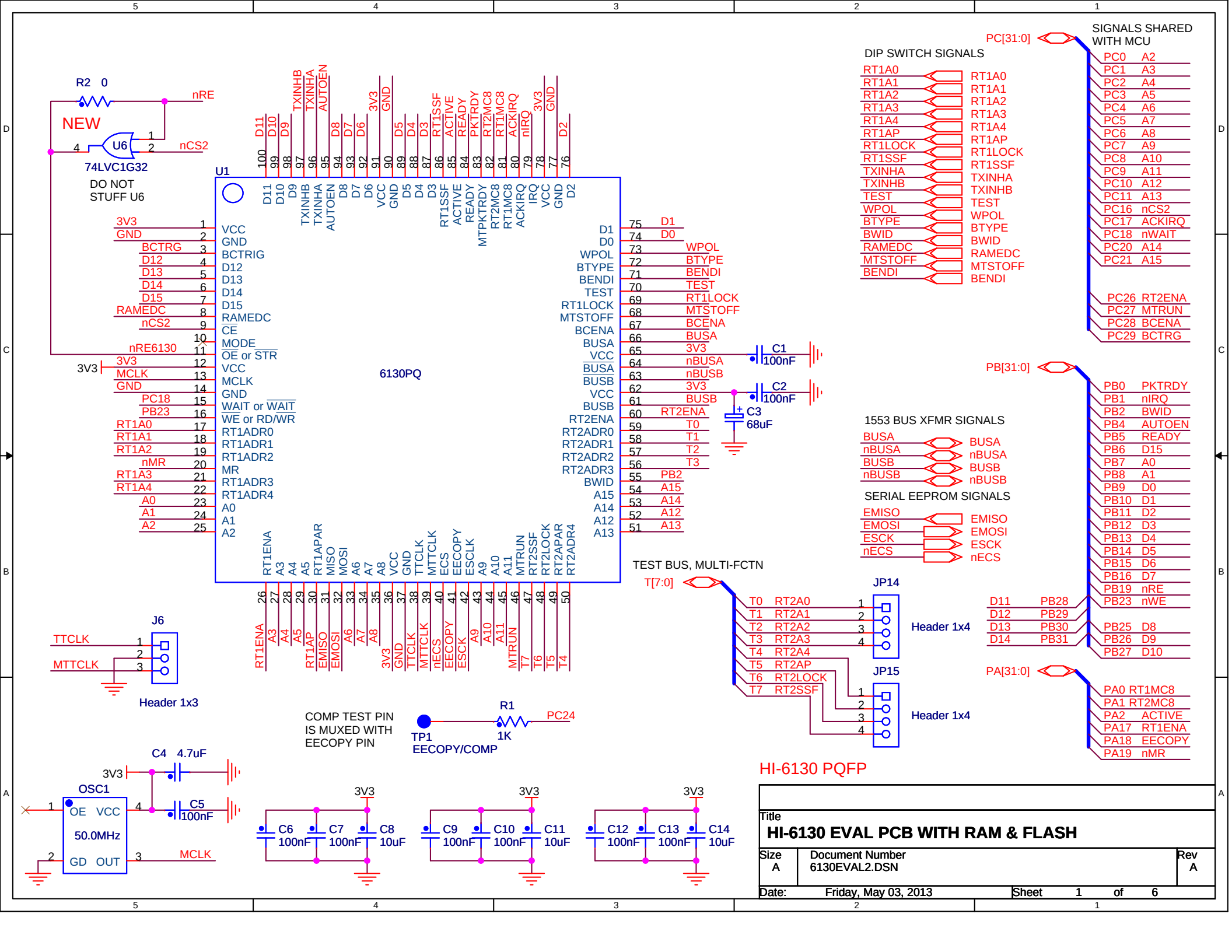


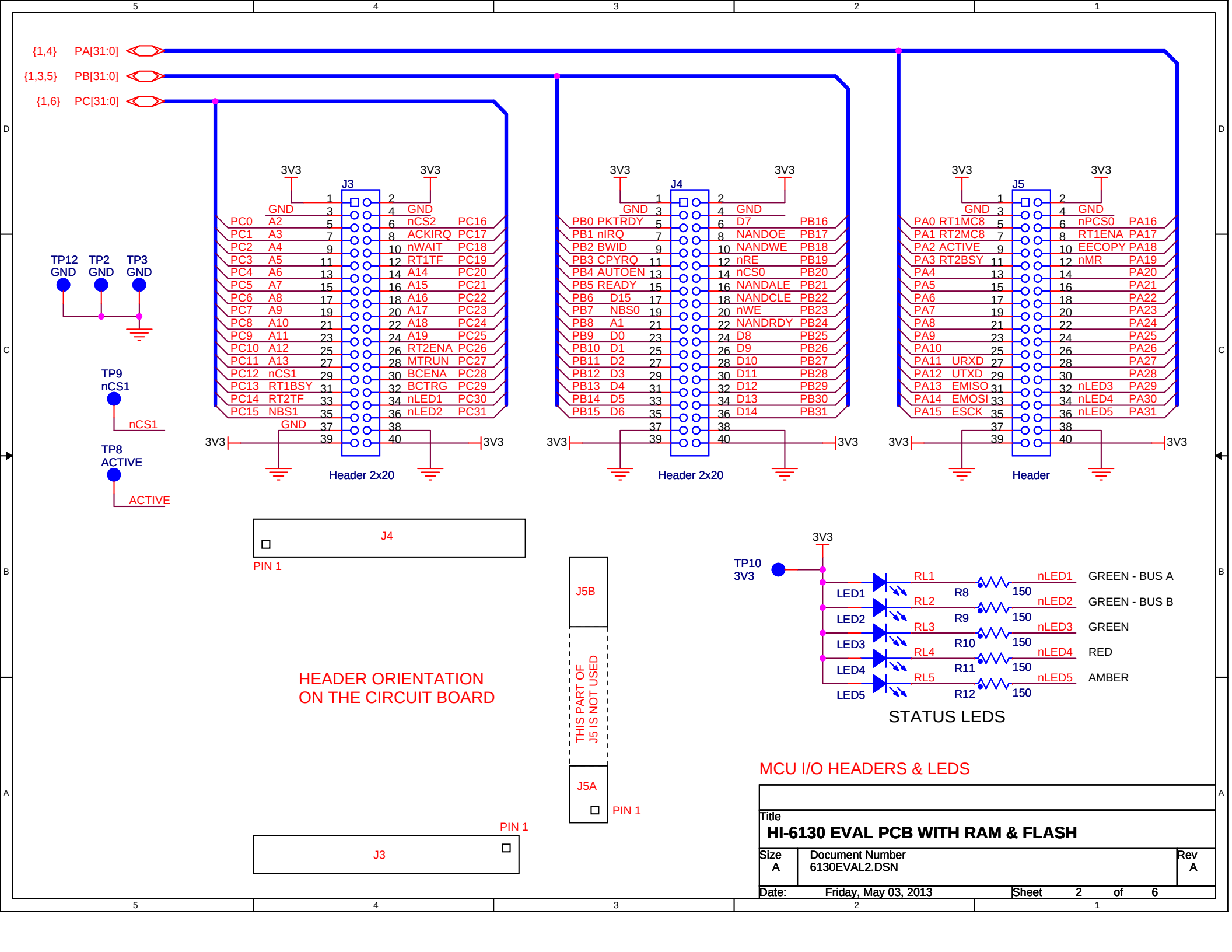


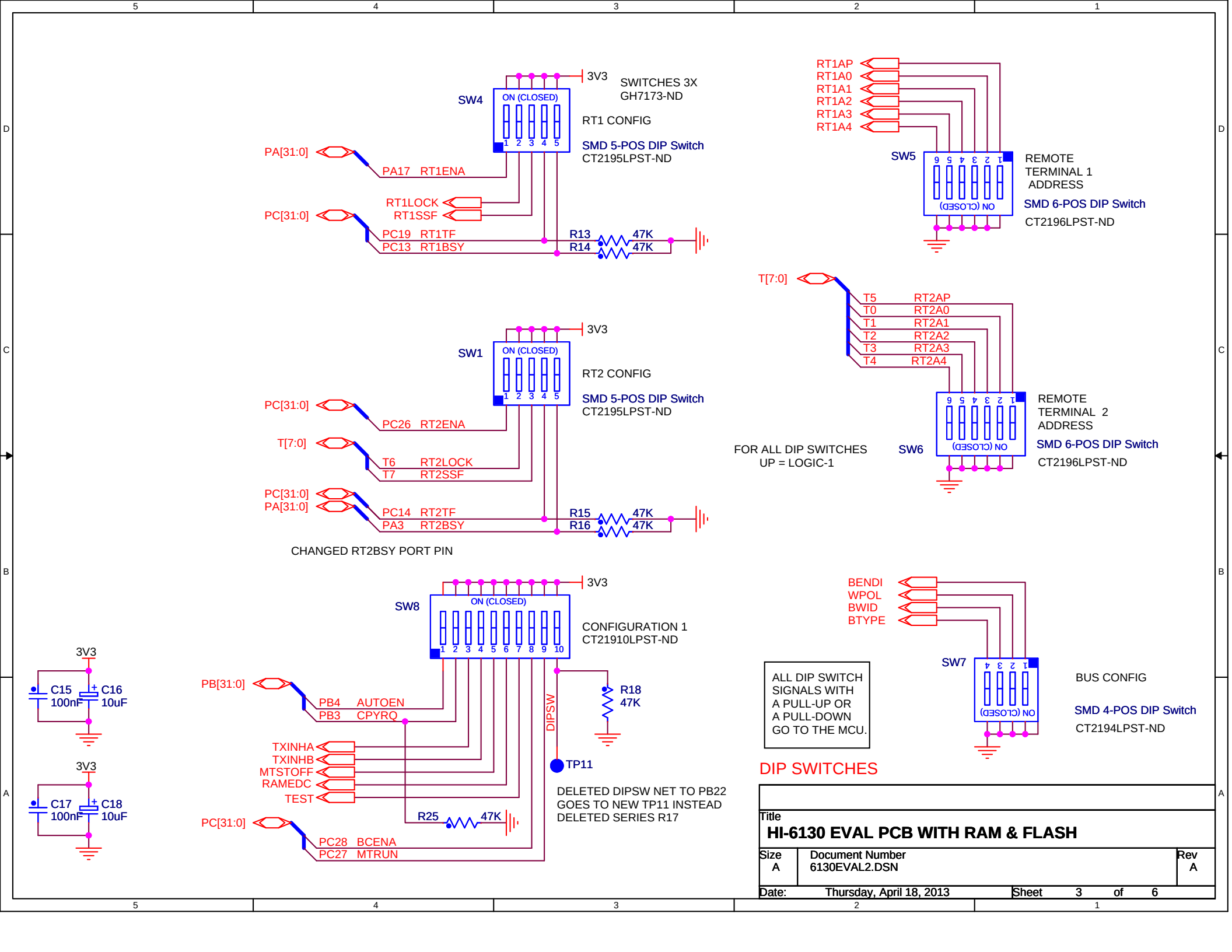
The separate Holt API users guide contains all the information necessary to use the API library functions.

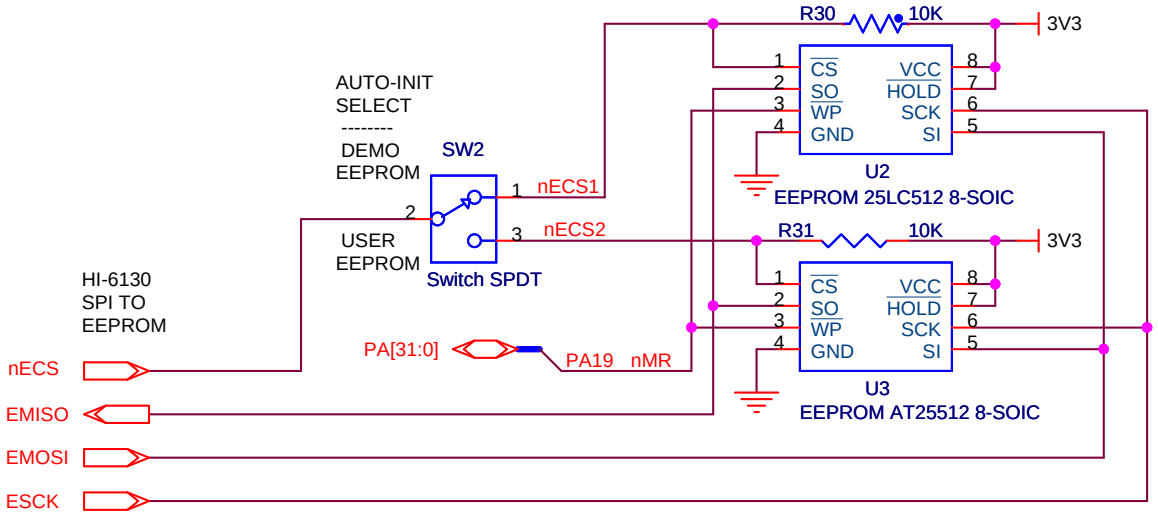
Evaluation board schematic diagrams and bills of material are provided on the following pages

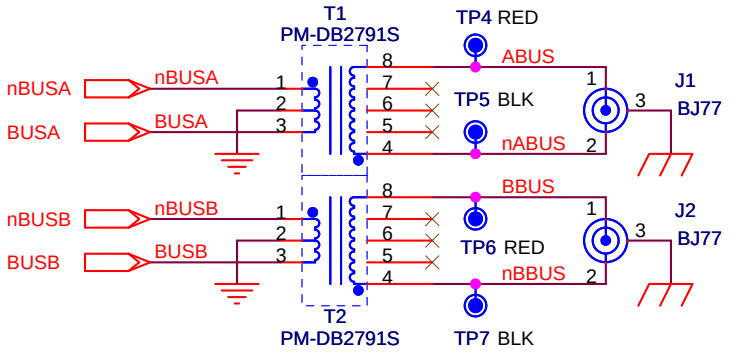
At the end of the document, memory maps show how RAM is allocated.

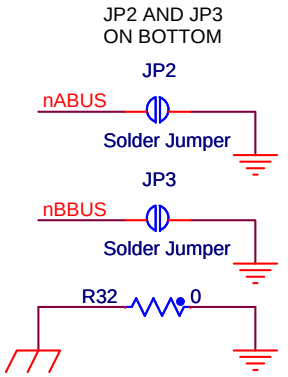

R2 0
nRE
NEW
U6
74LVC1G32
nCS2
DO NOT
STUFF U6
U1
6130PQ
nRE6130
3V3
MCLK
WAIT or WAIT
WE or RD/WR
MODE
OE or STR
MR
C1
100nF
C2
100nF
C3
68uF
SIGNALS SHARED
WITH MCU
PC[31:0]
DIP SWITCH SIGNALS
1553 BUS XFMR SIGNALS
SERIAL EEPROM SIGNALS
PB[31:0]
PA[31:0]
TEST BUS, MULTI-FCTN
T[7:0]
JP14
JP15
Header 1x4
J6
Header 1x3
COMP TEST PIN
IS MUXED WITH
EECOPY PIN
TP1
EECOPY/COMP
R1
1K
PC24
OSC1
50.0MHz
C4 4.7uF
C5
100nF
C6
100nF
C7
100nF
C8
10uF
C9
100nF
C10
100nF
C11
10uF
C12
100nF
C13
100nF
C14
10uF
HI-6130 PQFP
Title
HI-6130 EVAL PCB WITH RAM & FLASH
Size
A
Document Number
6130EVAL2.DSN
Rev
A
Date:
Friday, May 03, 2013
Sheet
1
of
6


{1,4} PA[31:0]
{1,3,5} PB[31:0]
{1,6} PC[31:0]
TP12 GND
TP2 GND
TP3 GND
TP9 nCS1
nCS1
TP8 ACTIVE
ACTIVE
J3
3V3
GND
PC0 A2
PC1 A3
PC2 A4
PC3 A5
PC4 A6
PC5 A7
PC6 A8
PC7 A9
PC8 A10
PC9 A11
PC10 A12
PC11 A13
PC12 nCS1
PC13 RT1BSY
PC14 RT2TF
PC15 NBS1
nCS2 PC16
ACKIRQ PC17
nWAIT PC18
RT1TF PC19
A14 PC20
A15 PC21
A16 PC22
A17 PC23
A18 PC24
A19 PC25
RT2ENA PC26
MTRUN PC27
BCENA PC28
BCTRG PC29
nLED1 PC30
nLED2 PC31
Header 2x20
J4
PB0 PKTRDY
PB1 nIRQ
PB2 BWID
PB3 CPYRQ
PB4 AUTOEN
PB5 READY
PB6 D15
PB7 NBS0
PB8 A1
PB9 D0
PB10 D1
PB11 D2
PB12 D3
PB13 D4
PB14 D5
PB15 D6
D7 PB16
NANDOE PB17
NANDWE PB18
nRE PB19
nCS0 PB20
NANDALE PB21
NANDCLE PB22
nWE PB23
NANDRDY PB24
D8 PB25
D9 PB26
D10 PB27
D11 PB28
D12 PB29
D13 PB30
D14 PB31
Header 2x20
J5
PA0 RT1MC8
PA1 RT2MC8
PA2 ACTIVE
PA3 RT2BSY
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11 URXD
PA12 UTXD
PA13 EMISO
PA14 EMOSI
PA15 ESCK
nPCS0 PA16
RT1ENA PA17
EECOPY PA18
nMR PA19
PA20
PA21
PA22
PA23
PA24
PA25
PA26
PA27
PA28
nLED3 PA29
nLED4 PA30
nLED5 PA31
Header
J4
PIN 1
J5B
THIS PART OF J5 IS NOT USED
J5A
PIN 1
HEADER ORIENTATION ON THE CIRCUIT BOARD
PIN 1
J3
TP10 3V3
LED1
LED2
LED3
LED4
LED5
RL1
RL2
RL3
RL4
RL5
R8
R9
R10
R11
R12
150
nLED1 GREEN - BUS A
nLED2 GREEN - BUS B
nLED3 GREEN
nLED4 RED
nLED5 AMBER
STATUS LEDS
MCU I/O HEADERS & LEDS
Title
HI-6130 EVAL PCB WITH RAM & FLASH
Size A
Document Number 6130EVAL2.DSN
Rev A
Date: Friday, May 03, 2013
Sheet 2 of 6


SW4
ON (CLOSED)
1 2 3 4 5
3V3
SWITCHES 3X
GH7173-ND
RT1 CONFIG
SMD 5-POS DIP Switch
CT2195LPST-ND
PA[31:0]
PA17 RT1ENA
PC[31:0]
RT1LOCK
RT1SSF
PC19 RT1TF
PC13 RT1BSY
R13 47K
R14 47K
RT1AP
RT1A0
RT1A1
RT1A2
RT1A3
RT1A4
SW5
REMOTE
TERMINAL 1
ADDRESS
SMD 6-POS DIP Switch
CT2196LPST-ND
SW1
RT2 CONFIG
SMD 5-POS DIP Switch
CT2195LPST-ND
PC26 RT2ENA
T[7:0]
T6 RT2LOCK
T7 RT2SSF
PC14 RT2TF
PA3 RT2BSY
R15 47K
R16 47K
CHANGED RT2BSY PORT PIN
T5 RT2AP
T0 RT2A0
T1 RT2A1
T2 RT2A2
T3 RT2A3
T4 RT2A4
SW6
REMOTE
TERMINAL 2
ADDRESS
SMD 6-POS DIP Switch
CT2196LPST-ND
FOR ALL DIP SWITCHES
UP = LOGIC-1
SW8
CONFIGURATION 1
CT21910LPST-ND
PB[31:0]
PB4 AUTOEN
PB3 CPYRQ
TXINHA
TXINHB
MTSTOFF
RAMEDC
TEST
PC28 BCENA
PC27 MTRUN
R25 47K
DIPSW
R18 47K
TP11
DELETED DIPSW NET TO PB22
GOES TO NEW TP11 INSTEAD
DELETED SERIES R17
C15 100nF
C16 10uF
C17 100nF
C18 10uF
BENDI
WPOL
BWID
BTYPE
SW7
BUS CONFIG
SMD 4-POS DIP Switch
CT2194LPST-ND
ALL DIP SWITCH
SIGNALS WITH
A PULL-UP OR
A PULL-DOWN
GO TO THE MCU.
DIP SWITCHES
Title
HI-6130 EVAL PCB WITH RAM & FLASH
Size A
Document Number
6130EVAL2.DSN
Rev A
Date: Thursday, April 18, 2013
Sheet 3 of 6

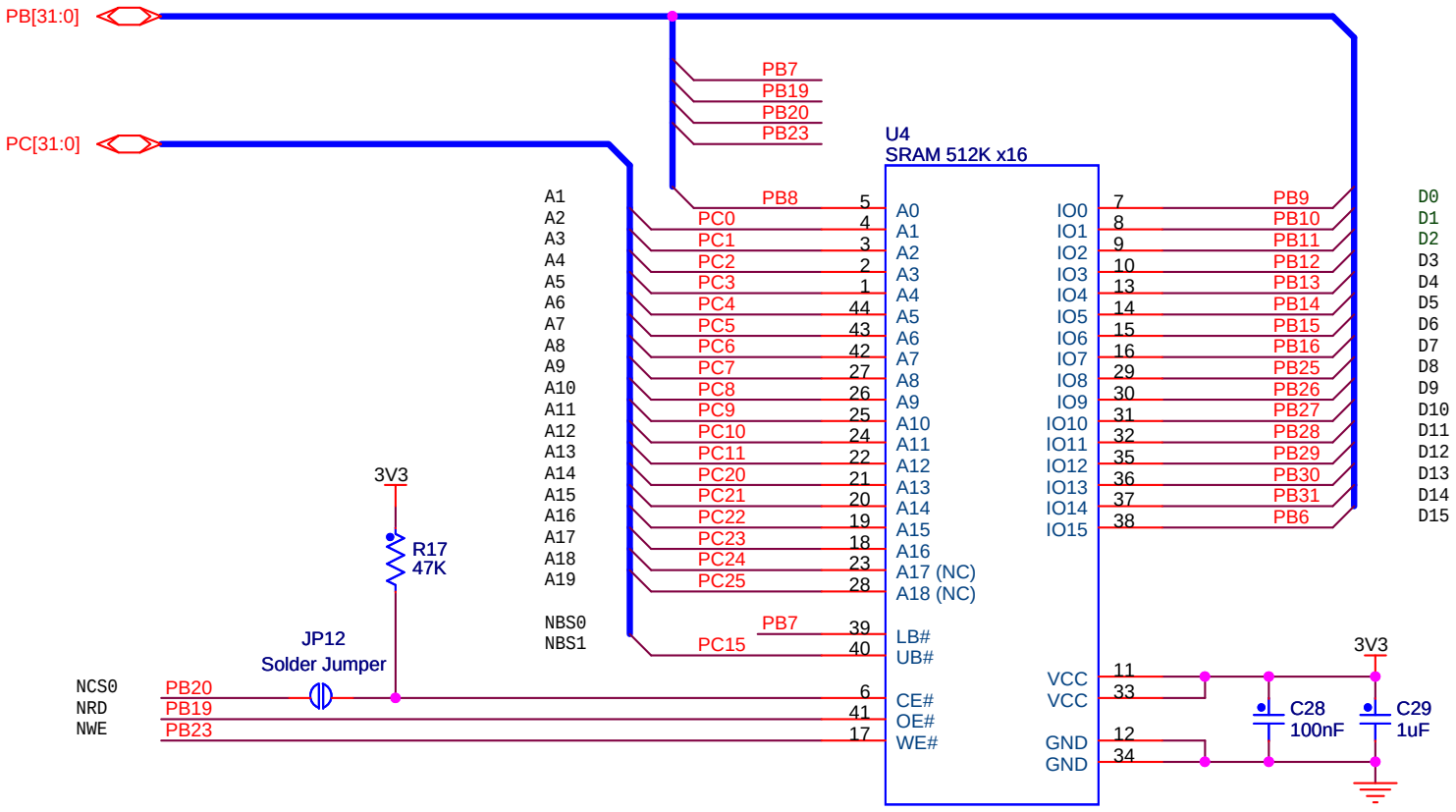






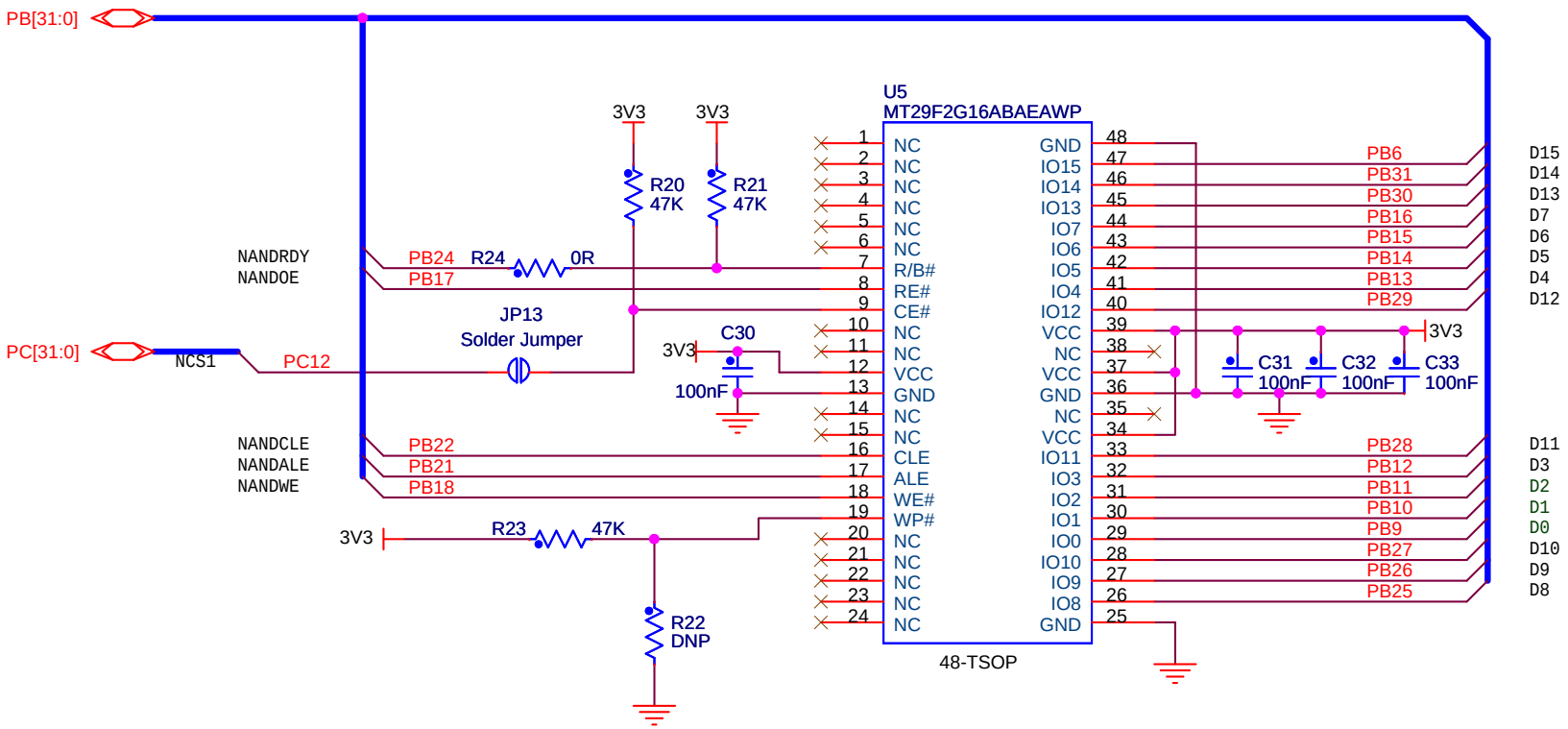
EEPROM, 1553 BUS

Title: **HI-6130 EVAL PCB WITH RAM & FLASH**		
Size: A	Document Number: 6130EVAL2.DSN	Rev: A
Date: Friday, May 03, 2013	Sheet 4 of 6	



128K x16 SRAM

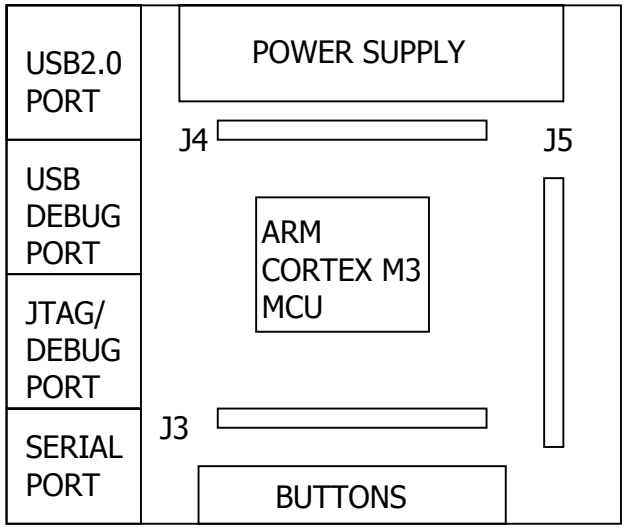
Title: **HI-6130 EVAL PCB WITH RAM & FLASH**		
Size: A	Document Number: 6130EVAL2.DSN	Rev: A
Date: Friday, May 03, 2013	Sheet 5 of 6	



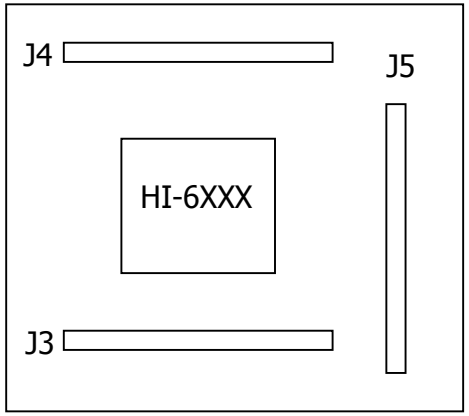
128K x16 NAND FLASH

Title: **HI-6130 EVAL PCB WITH RAM & FLASH**		
Size: A	Document Number: 6130EVAL2.DSN	Rev: A
Date: Friday, May 03, 2013	Sheet 6 of 6	

Bill of Materials		HI-6130-2 (RAM & FLASH) Evaluation Board, Top			Oct. 3, 2013
Item	***Qty***	***Description***	***Reference***	***DigiKey***	***Mfr P/N***
1	1	PCB, Bare, Eval Board	N/A	--------	--------
2	16	Capacitor, Ceramic 0.1uF 20% 50V Z5U 0805	C1,C2,C5, C6,C7,C9, C10,C12,C13, C15,C17,C28,C30, C31,C32,C33	399-1176-1-ND	Kemet C0805C104M5UACTU
3	1	Capacitor, Ceramic 1uF 10% 16V X5R 0805	C29	399-8005-1-ND	Kemet C0805C105K4PACTU
4	5	Capacitor, Ceramic 10uF 10% 6.3V X5R 0805	C8,C11,C14, C16,C18	399-3138-1-ND	Kemet C0805C106K9PACTU
5	1	Capacitor 68uF 10% 6.3V Tantalum 400 mOhm SMD EIA 6032-28	C3	495-1507-1-ND	Kemet B45197A1686K309
6	2	Connector 3-Lug Concentric Triax Bayonet Jack, Panel Front Mount TRB (BJ77)	J1,J2	MilesTek 10-06570	Trompeter Electronics BJ77 Use 0.469" Round Hole
7	2	Header, Male 2x20 0.1" Pitch, 0.230" Pins, 0.120" Tails	J3,J4	S2012E-20-ND	Sullins
8	1	Header, Male 2x4 0.1" Pitch, 0.230" Pins, 0.120" Tails	J5A	S2012E-04-ND	Sullins
9	1	Header, Male 2x5 0.1" Pitch, 0.230" Pins, 0.120" Tails	J5B	S2012E-05-ND	Sullins
10	------	Header, 1x3, 0.1" pitch	J6	DO NOT STUFF	--------
11	------	Header, 1x8, 0.1" pitch	J7	DO NOT STUFF	--------
12	1	Header, 4x3, 0.1" pitch	JP1	Samtec	Samtec TSW-104-07-T-T
13	4	Jumper, shorting, w/ grip, 0.1"	JP1	S9341-ND	Sullins NPC02SXON-RC
14		Solder Jumper	JP2,JP3	DO NOT SOLDER	--------
15	1	LED Yellow 0805	LED5	160-1175-1-ND	Lite On LTST-C170YKT
16	3	LED Green 0805	LED1 - LED3	160-1179-1-ND	LiteOn LTST-C170GKT
17	1	LED Red 0805	LED4	160-1176-1-ND	LiteOn LTST-C170CKT
18	1	Osc, 50.00MHz 25ppm 3.3V SMD 5mm x 7mm	OSC1	CTX327LVCT-ND	CTX CB3LV-3I-50M0000-T
19	2	Resistor, 0 Ohm 0805	R17,R32	P0.0ACT-ND	Any
20	5	Resistor, 150 5% 1/8W 0805	R8,R9,R10, R11,R12	P150ACT-ND	Any
21	1	Resistor, 1.0K 5% 1/8W 0805	R1	P1.0KACT-ND	Any
22	2	Resistor, 10K 5% 1/8W 0805	R30,R31	P10KACT-ND	Any
23	10	Resistor, 47K 5% 1/8W 0805	R13,R14,R15 R16,R17,R18,R20, R21,R23,R25	P47KACT-ND	Any
24	1	DIP Switch 4-Position SMD	SW7	CT2194LPST-ND	CTS 219-4LPST
25	2	DIP Switch 5-Position SMD	SW1,SW4	CT2195LPST-ND	CTS 219-5LPST
26	2	DIP Switch 6-Position SMD	SW5,SW6	CT2196LPST-ND	CTS 219-6LPST
27	1	DIP Switch 10-Position SMD	SW8	CT21910LPST-ND	CTS 219-10LPST
28	1	Slide Switch SPDT SMD	SW2	563-1022-1-ND	Copal CJS-1200TB
29	2	Transformer MIL-STD-1553 Single, 1:2.50, PM-DB2791S	T1,T2	Holt PM-DB2791S	Premier Magnetics PM-DB2791S
30	------	Test Point, pad w/ plated hole	TP1,TP9,TP10	------	--------
31	2	Test Point, Red Insulator, 0.062" hole	TP4,TP6	5010K-ND	Keystone 5010
32	3	Test Point, Black Insulator, 0.062" hole	TP2,TP3,TP5, TP7	5011K-KD	Keystone 5011
33	1	Test Point, White Insulator, 0.062" hole	TP8	5012K-KD	Keystone 5012
34	1	IC HI-6130 Holt 100-PQFP	U1	------	--------
35	2	IC, Serial EEPROM 512Kbit 20MHz SPI 8-SOIC, Microchip	U2, U3	25LC512T-I/SNCT-ND	Microchip 25LC512T-I/SN
35	1	IC, SRAM 512K x 16	U4	CY62136FV30LL-45ZSXI-ND	Cypress CY62136FV30LL-45ZSXI
36	1	IC, FLASH NAND	U5	557-1613-ND	Micron MT29F2G16ABAEAWP-IT:E



LOWER CIRCUIT BOARD



STACKING UPPER CIRCUIT BOARD

J3,J4 & J5 ARE DUAL-ROW STACKING RECEPTACLES (LOWER BOARD) AND HEADERS (UPPER BOARD).

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
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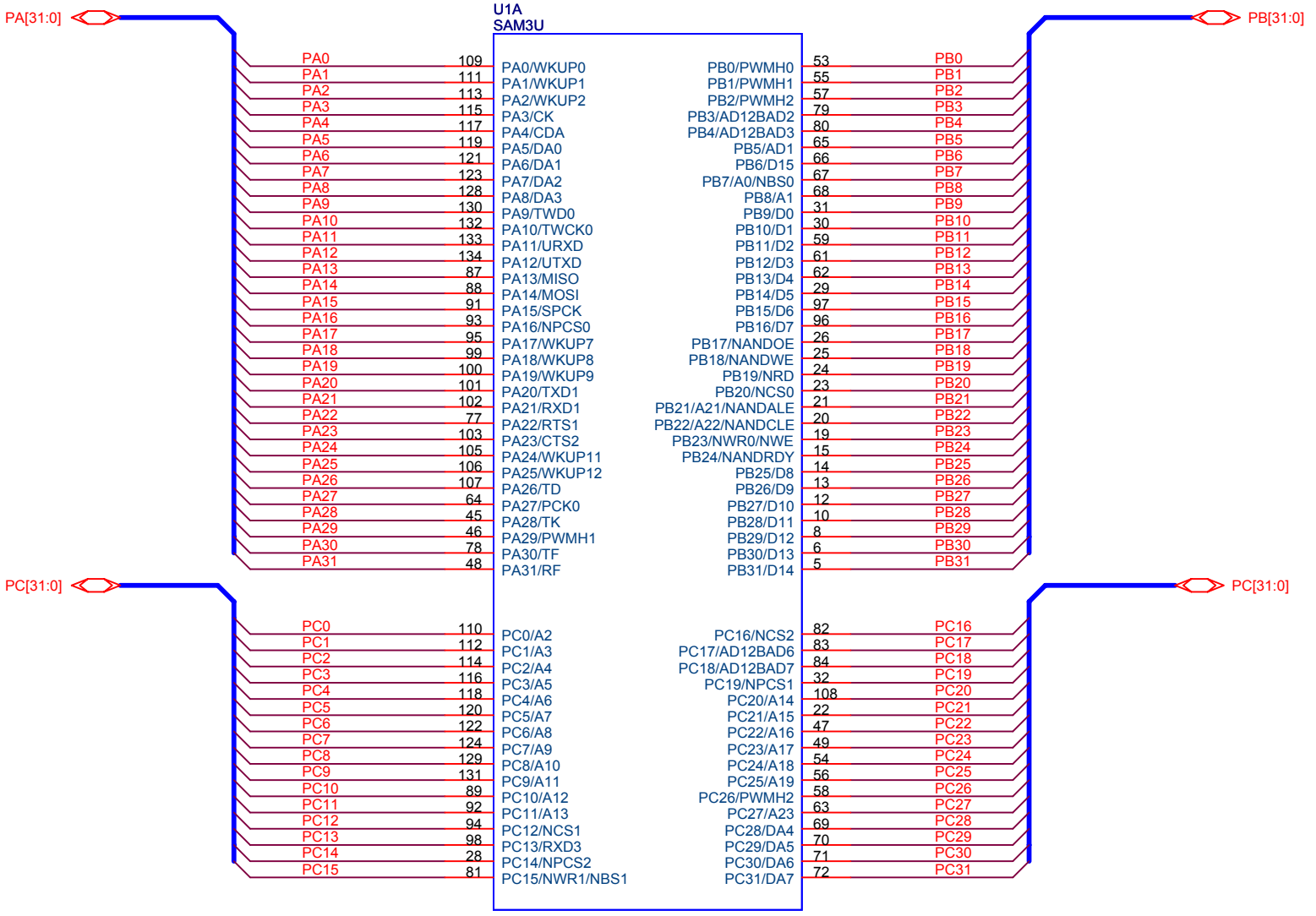
BUTTONS



ARM CORTEX M3 PIO

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
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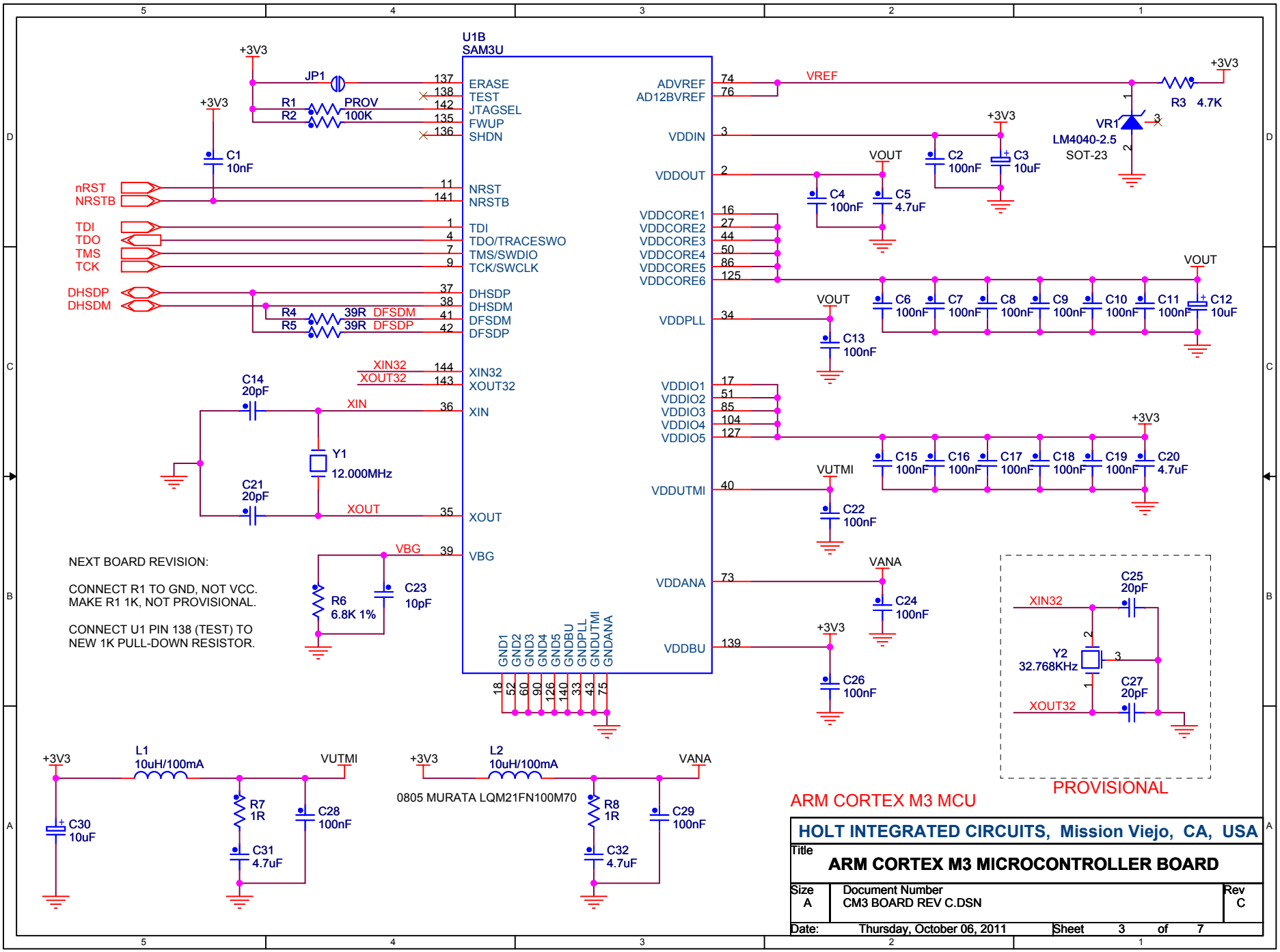
U1B
SAM3U
+3V3
JP1
R1
R2
PROV
100K
C1
10nF
nRST
NRSTB
TDI
TDO
TMS
TCK
DHSDP
DHSDM
R4
R5
39R DFSDM
39R DFSDP
C14
20pF
C21
20pF
XIN32
XOUT32
XIN
XOUT
Y1
12.000MHz
VBG
R6
6.8K 1%
C23
10pF
NEXT BOARD REVISION:
CONNECT R1 TO GND, NOT VCC.
MAKE R1 1K, NOT PROVISIONAL.
CONNECT U1 PIN 138 (TEST) TO
NEW 1K PULL-DOWN RESISTOR.
ERASE
TEST
JTAGSEL
FWUP
SHDN
NRST
NRSTB
TDI
TDO/TRACESWO
TMS/SWDIO
TCK/SWCLK
DHSDP
DHSDM
DFSDM
DFSDP
XIN32
XOUT32
XIN
XOUT
VBG
GND1
GND2
GND3
GND4
GND5
GNDBU
GNDPLL
GNDUTMI
GNDANA
ADVREF
AD12BVREF
VDDIN
VDDOUT
VDDCORE1
VDDCORE2
VDDCORE3
VDDCORE4
VDDCORE5
VDDCORE6
VDDPLL
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDUTMI
VDDANA
VDDBU
VREF
R3 4.7K
VR1
LM4040-2.5
SOT-23
C2 100nF
C3 10uF
C4 100nF
C5 4.7uF
C6 100nF
C7 100nF
C8 100nF
C9 100nF
C10 100nF
C11 100nF
C12 10uF
C13 100nF
C15 100nF
C16 100nF
C17 100nF
C18 100nF
C19 100nF
C20 4.7uF
C22 100nF
C24 100nF
C26 100nF
VOUT
VUTMI
VANA
L1
10uH/100mA
L2
10uH/100mA
0805 MURATA LQM21FN100M70
C30
10uF
R7
1R
C28
100nF
C31
4.7uF
R8
1R
C29
100nF
C32
4.7uF
C25
20pF
Y2
32.768KHz
C27
20pF
PROVISIONAL
ARM CORTEX M3 MCU
HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA
Title
ARM CORTEX M3 MICROCONTROLLER BOARD
Size
A
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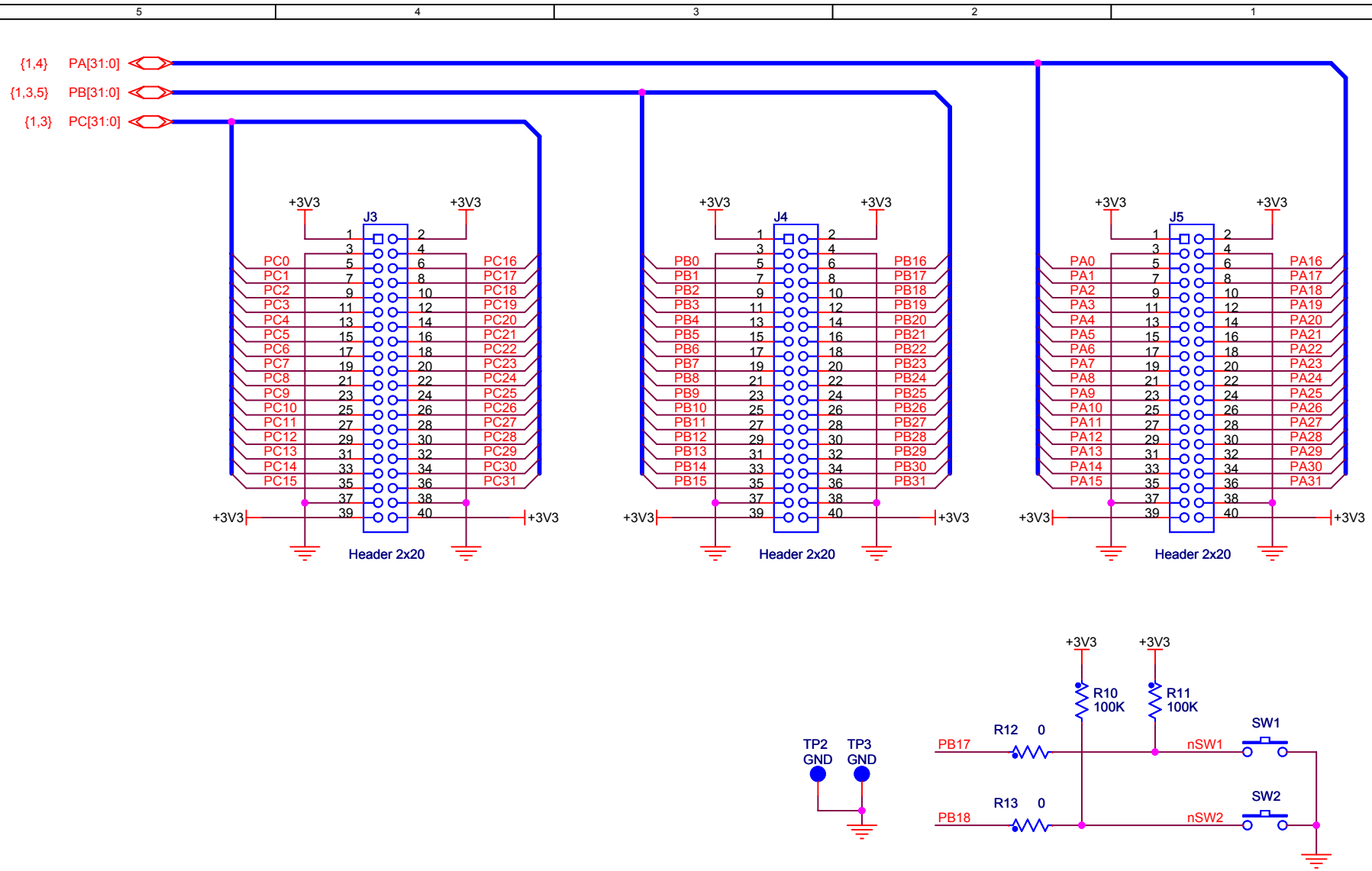

BOARD I/O HEADERS, BUTTONS

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
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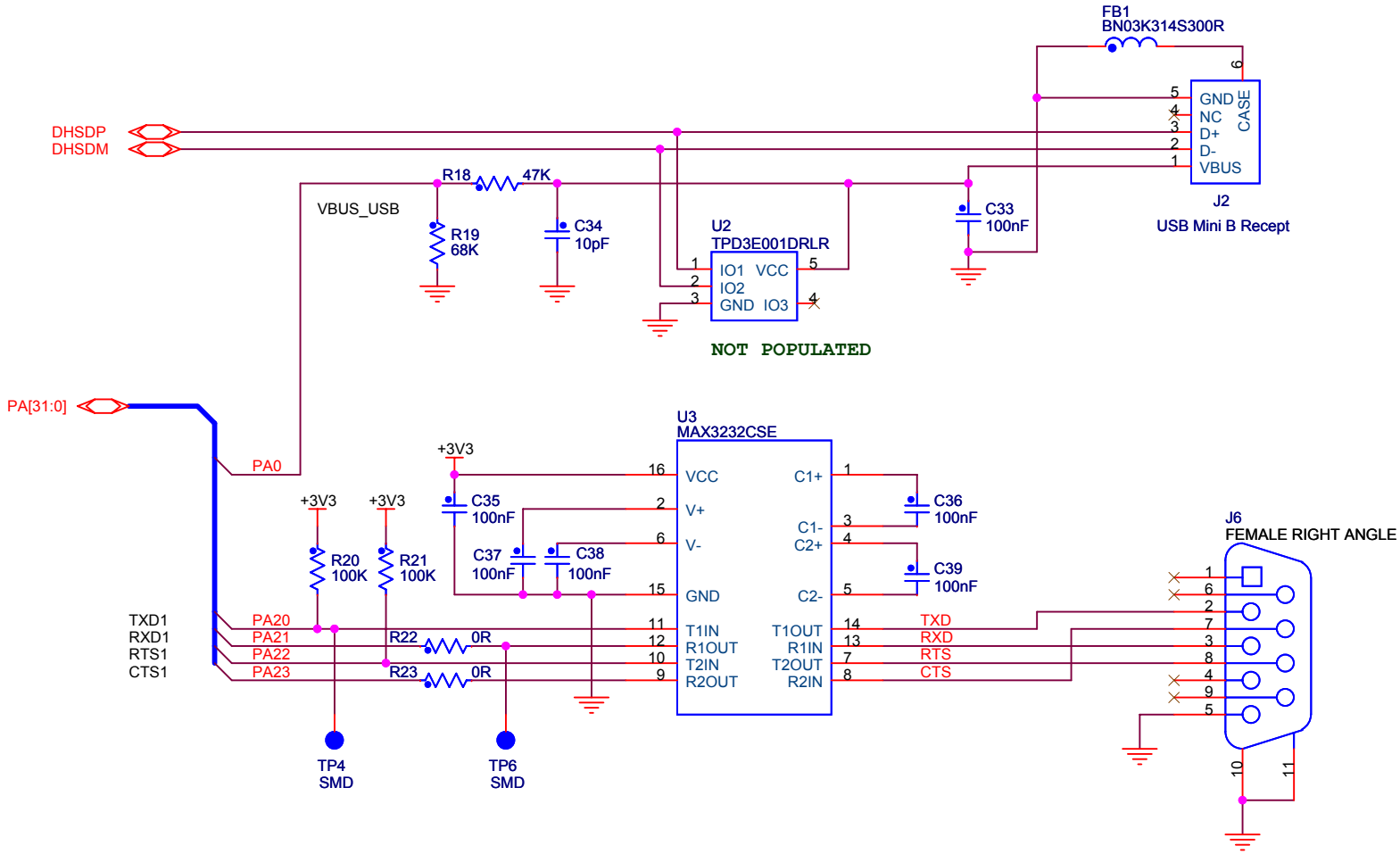

USB & RS-232 SERIAL

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
Title: ARM CORTEX M3 MICROCONTROLLER BOARD		
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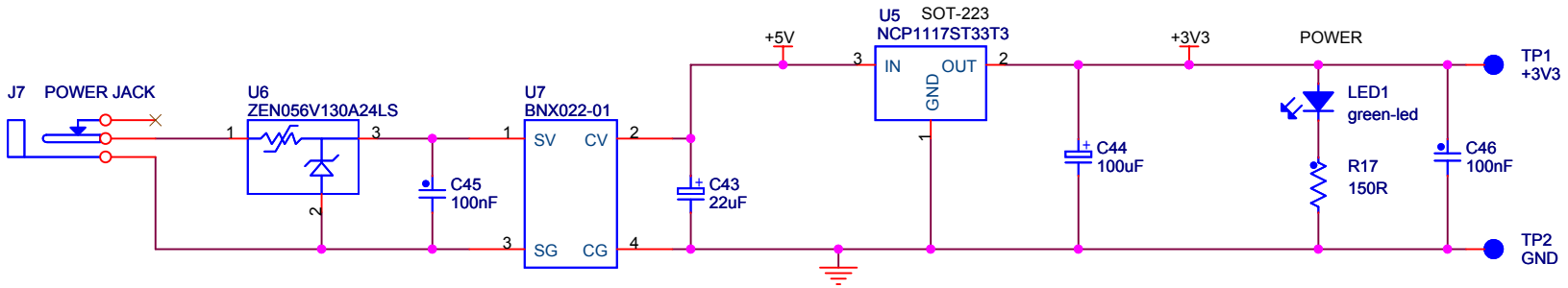

POWER SUPPLY

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
Title: ARM CORTEX M3 MICROCONTROLLER BOARD		
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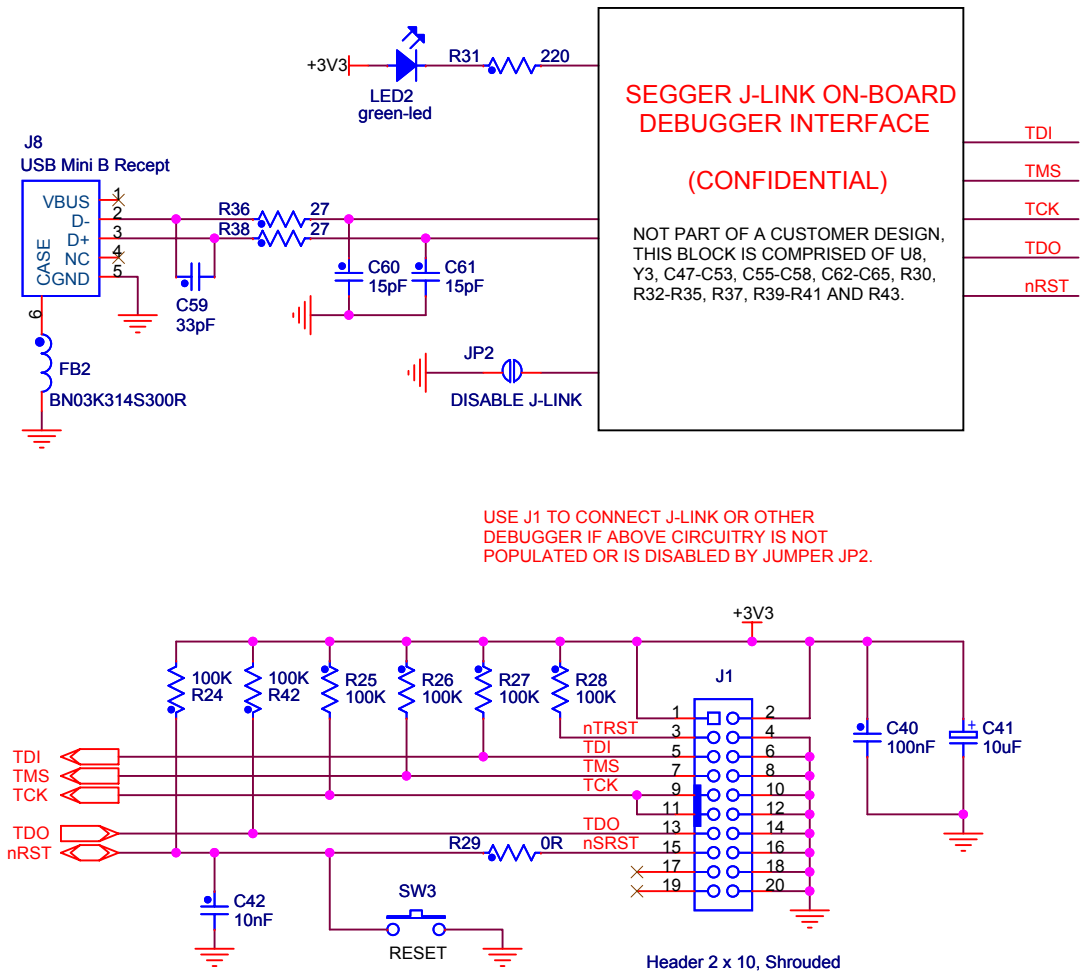

DEBUG INTERFACE

HOLT INTEGRATED CIRCUITS, Mission Viejo, CA, USA		
Title: ARM CORTEX M3 MICROCONTROLLER BOARD		
Size: A	Document Number: CM3 BOARD REV C.DSN	Rev: C
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Bill of Materials		ARM Cortex M3 MCU Board			Revised: 9 Sept 2011
Item	*Qty*	*Description*	*Reference*	*DigiKey*	*Mfr P/N*
1	1	PCB, Bare, Evaluation Board, revision B or C	N/A	--------	
2	1	Ferrite Bead, 220 Ohm @ 100MHz 300mA DC 0805	FB1	732-1602-1-ND	Wurth 742792034
3	2	Capacitor, Ceramic 10nF 10% 50V X7R 0805	C1,C42	399-1158-1-ND	Kemet C0805C103K5RACTU
4	2	Capacitor, Ceramic 10pF 10% NP0 C0G 0V 0805	C23,C34	478-3731-1-ND	AVX 080551A100KAT2A
5	4	Capacitor, Ceramic 20pF 5% NP0 C0G 0V 0805	C14,C21,C25, C27	478-3735-1-ND	AVX 080551A200JAT2A
6	28	Capacitor, Ceramic 100nF 20% 50V Z5U 0805	C2,C4,C6-C11, C13,C15-C19, C22,C24,C26, C28,C29,C33, C35-C40,C45-46	399-1176-1-ND	Kemet C0805C104M5UACTU
7	4	Capacitor, Tantalum 4.7uF 10% 10V Low ESR SMD 1206	C5,C20,C31, C32	478-2391-11-ND	AVX TPSA475K010R1400
8	4	Capacitor, Tantalum 10uF 10% 10V Low ESR SMD 1206	C3,C12,C30,C41	478-3317-1-ND	AVX TPSA106K010R1800
9	1	Capacitor 22uF 10% 6.3V Tantalum Low ESR SMD C	C43	495-1504-1-ND	Kemet B45197A1226K309
10		Capacitor 100uF 10% 6.3V Tantalum Low ESR SMD C	C44	495-1509-1-ND	Kemet B45197A1107K309
11	1	Header, Male Shrouded 2x10 0.1" Pitch	J1	MHB20K-ND	3M 2520-6002UB
12	1	Connector, Receptacle USB Mini B Rt-Angle PCB Mount	J2	H2959CT-ND	Hirose UX60-MB-5ST
13	1	Connector DB9F, Right-Angle PCB Short Body, Board Lock	J6	182-109FE-ND	NorComp 182-009-213R-561
14	1	Jack, DC Power, 2.5mm ID x 2.1mm pin	J7	CP-102AH-ND	CUI PJ-102AH
15	2	Receptacle, Female 2x20 0.1" Pitch, 8.5mm Height, 3.2mm Solder Tails	J3,J4	S6104-ND	Sullins PPTC202LFBN-RC
16	1	Receptacle, Female 2x4 0.1" Pitch, 8.5mm Height, 3.2mm Solder Tails	J5A (J5 lower end, close to Bus B)	S7072-ND	Sullins PPTC042LFBN-RC
17	1	Receptacle, Female 2x5 0.1" Pitch, 8.5mm Height, 3.2mm Solder Tails	J5B (J5 upper end, close to Bus A)	S6105-ND	Sullins PPTC052LFBN-RC
18	1	Solder Jumper	JP1	SOLDER CLOSED	
19	2	Inductor, 10uH, 100mA 0805	L1,L2	490-4029-1-ND	Murata LQM21FN100M70L
20	1	LED Green 0805	LED1	160-1179-2-ND	LiteOn LTST-C170GKT
21	0	Resistor, Prov 1/8W 0805	R1	DO NOT STUFF	
22	5	Resistor, 0 ohm 1/8W 0805	R12,R13,R22, R23,R29	311-0ARCT-ND	Panasonic ERJ-6GEY0R00V
23	2	Resistor, 1.0 5% 1/8W 0805	R7,R8	P1.0ACT-ND	Panasonic ERJ-6GEYJ1R0V
24	2	Resistor, 39 5% 1/8W 0805	R4,R5	P39ACT-ND	Panasonic ERJ-6GEYJ390V
25	1	Resistor, 150 5% 1/8W 0805	R17	P150ACT-ND	Panasonic ERJ-6GEYJ151V
26	1	Resistor, 4.7K 5% 1/8W 0805	R3	P4.7KACT-ND	Panasonic ERJ-6GEYJ472V
27	1	Resistor, 6.8K 5% 1/8W 0805	R6	P6.8KACT-ND	Panasonic ERJ-6GEYJ682V
28	1	Resistor, 47K 5% 1/8W 0805	R18	P47KACT-ND	Panasonic ERJ-6GEYJ473V
29	1	Resistor, 68K 5% 1/8W 0805	R19	P68KACT-ND	Panasonic ERJ-6GEYJ683V
30	10	Resistor,100K 5% 1/8W 0805	R2,R10,R11, R20,R21,R24, R25,R26,R27, R28	P100KACT-ND	Panasonic ERJ-6GEYJ104V
31	3	Pushbutton	SW1,SW2,SW3	P10886SCT-ND	Panasonic EVQ-QWS02W
32	2	Test Point, Black Insulator, 0.062" hole	TP2,TP3	5011K-KD	Keystone 5011

33	1	Test Point, Orange Insulator, 0.062" hole	TP1	5008K-ND	Keystone 5008
34	1	Test Point, Yellow Insulator, 0.062" hole	TP4	5009K-ND	Keystone 5009
35	2	Test Point, Hole / Pad Only	TP5,TP6		
36	1	IC, MCU 32-Bit 256KB Flash, 144-LQFP	U1	ATSAM3U4EA-AU-ND	Atmel ATSAM3U4EA-AU
37	1	IC, ESD Protection Array 3-Channel SOT-5	U2	296-21885-1-ND	Texas Inst TPD3E001DRLR
38	1	IC, RS232 Driver/Receiver 3.0 to 5.5VDC 16-SOIC (3.9mm wide)	U3	296-19752-1-ND	Texas Inst MAX3232EIDR
39	1	IC, Single Inverter 74LVC1G04 SC70-05	U4	296-11600-1-ND	Texas Inst SN74LVC1G04DCKR
40	1	IC Voltage Regulator 3.3V 1A LDO, SOT-223	U5	497-1228-1-ND	ST Micro LD1117AS33TR
41	1	PolyZen 5.6V PPTC protected Zener SMD	U6	ZEN056V130A24LSCT-ND	Tyco ZEN056V130A24LS
42	1	Filter, EMI 35dB 10A 1MHz-1GHz SMD	U7	490-5052-1-ND	Murata BNX022-01L
43	1	IC Voltage Ref 2.5V 1% Micropower SOT-23	VR1	576-1047-1-ND	Micrel LM4040DYM3-2.5
44	1	Crystal 12.00MHz, 50ppm 20pF, HC-49US leaded	Y1	631-1105-ND	Fox FOXSLF/120-20
45	1	Crystal, 32768 Hz 12.5pF cylinder leaded	Y2	535-9033-1-ND	Abracon AB26TRB-32.768KHZ-T
		J-Link On-Board Circuitry…			
46	10	Capacitor, Ceramic 100nF -20% / +80% 25V Y5V 0603	C48-C53, C55-C58	490-1575-1-ND	Murata GRM188F51E104ZA01D
47	1	Capacitor, Ceramic 33pF 5% 50V C0G 0603	C59	490-1415-1-ND	Murata GRM1885C1H330JA01D
48	2	Capacitor, Ceramic 15pF 5% 50V C0G 0603	C60,C61	490-1407-1-ND	Murata GRM1885C1H150JA01D
49	2	Capacitor, Ceramic 10pF 5% 50V C0G 0603	C62,C63	490-1403-1-ND	Murata GRM1885C1H100JA01D
50	1	Capacitor, Ceramic 1nF 20% 50V X7R 0603	C64	490-1495-1-ND	Murata GRM188R71H102MA01D
51	1	Capacitor, Ceramic 10nF 10% 50V X7R 0603	C65	490-1512-1-ND	Murata GRM188R71H103KA01D
52	1	Capacitor, Ceramic 4.7uF -20% / +80% 6.3V 0603	C47	587-1313-1-ND	Taiyo Yuden JMK212F475ZD-T
53	1	Ferrite Bead, 220 Ohm @ 100MHz 300mA DC 0805	FB2	SAME AS FB2 ABOVE	
54	1	Solder Jumper	JP2	LEAVE OPEN	
55	1	Connector, Receptacle USB Mini B Rt-Angle PCB Mount	J8	SAME AS J2 ABOVE	
56	1	LED Green 0805	LED2	SAME AS LED1 ABOVE	
57	1	Resistor, 0 ohm 1/10W 0603	R30	P0.0GCT-ND	Panasonic ERJ-3GEY0R00V
58	1	Resistor, 220 ohm 5% 1/10W 0603	R31	P220GCT-ND	Panasonic ERJ-3GEYJ221V
59	2	Resistor, 1.5K ohm 5% 1/10W 0603	R32,R41	P1.5KGCT-ND	Panasonic ERJ-3GEYJ152V
60	1	Resistor, 47K ohm 5% 1/10W 0603	R33	P47KGCT-ND	Panasonic ERJ-3GEYJ473V
61	1	Resistor, 100 ohm 5% 1/10W 0603	R34,R35,R37 R39	P100GCT-ND	Panasonic ERJ-3GEYJ101V
62	1	Resistor, 27 ohm 5% 1/10W 0603	R36,R38	P27GCT-ND	Panasonic ERJ-3GEYJ270V
63	1	Resistor, 300 ohm 5% 1/10W 0603	R40	P300GCT-ND	Panasonic ERJ-3GEYJ301V
64	1	IC AT91SAM7S64 64-PQFP programmed by Segger	U8	from Segger	
65	1	Crystal 18.432MHz, 30ppm 10pF, SMD 3.2x2.5 mm	Y3	535-10909-1-ND	Abracon ABM8G-18.432MHZ-4Y-T3

REVISION HISTORY

Document	Rev	Date	Description
AN-6132-2	New	10/10/13	Initial Release
	A	11/09/15	Updated for Demo Kit API Software Rev. 2.0B
	B	12/12/18	Rename API Library file to coincide with software update. HI-613x API LIB.a