HOLT INTEGRATED CIRCUITS INC.

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Frequently Asked Questions about the HI-8282 & HI-8382 Applications Note

Purpose

The primary purpose of this application note is to describe in detail some of the operations of the HI-8282 and the HI-8382 ARINC 429 devices. It is also intended to aid the user in avoiding some of the more common mistakes made in applying the devices.

With the above purpose in mind, the following are answers to some of the most commonly asked questions by engineers designing the chips into their system.

Questions

Question #1:

With an external loopback on the HI-8282 I never get a data ready flag from the receiver(s). Why?

Answer:

There are a variety of reasons as to why this can happen. Some of the more common causes are outlined below:

A.

The point of feedback is taken from the TTL outputs of the HI-8282, instead of from the driver outputs.

B.

The user has placed some sort of voltage level translating circuitry between the ARINC bus and the receiver inputs. No external level shifting is necessary, as the HI-8282 does this internally. If an external level shift is done, then the error detection circuitry inside the chip will interpret the incoming bits as invalid ARINC data and the $\overline{D/R}$ flag will not go low.

C.

The user has enabled the SDI bits in the control word register and the incoming SDI bits of the ARINC word do not match those programmed into the control word register. The user should either disable the SDI comparison function or make sure that the SDI bits programmed into the register match those of the word being transmitted.

D.

The data rate programmed into the control word register for the transmitter and the receiver are different. If the data rate of the word being transmitted is different from that of the receiver, then the error detection circuitry will ignore the word. The user should program the control word register so that both receiver and transmitter are operating at the same speed.

Question #2:

I have loaded the HI-8282 transmitter FIFO and enabled transmission (ENTX = “High"), but transmission begins and then suddenly stops for no apparent reason. What's wrong?

Answer:

The user is pulsing ENTX, rather than holding it high until the FIFO is completely empty and the TX/R line returns high.

Question #3:

May I tie the ENTX input of the HI-8282 to a One permanently?

Answer:

Yes. With this method, as soon as the first word is loaded into the FIFO, transmission will begin. During transmission of the first word, another seven words may be loaded into the FIFO. No loading of the FIFO should occur after transmission of the second word has begun.

Question #4:

If I tie ENTX permanently to a One, how will I know when transmission is complete?

Answer:

The Transmitter Ready Flag (TX/R) will go high.

Question #5:

Will I have enough time to load another seven words into the FIFO during transmission of the first word with ENTX tied high?

Answer:

In virtually all applications, the answer is yes. The user has 320 µs with high speed operation and 2.21 to 2.66 ms with low speed operation in which to load the remaining seven words. Most microprocessors operate at sufficient speed to accommodate the loading of the next seven words.

Question #6:

During external or internal loopback with the HI-8282, I can't clear the receiver Data Ready flag. What's causing this?

Answer:

This is usually caused by the user only retrieving one byte of the ARINC word. This $\overline{D/R}$ flag is only reset when the entire ARINC word has been retrieved.

Question #7:

Can the HI-8282 be used with ARINC 575?

Answer:

Yes. The chip meets all requirements of the ARINC 575 specification; however, one requirement of this specification requires some additional software overhead.

ARINC 575 allows the 32nd data bit of the ARINC word to be selectable as either parity or data. The transmitter circuitry of the HI-8282 automatically generates parity for each word transmitted. The 32nd bit of the transmitted word can be set to either a one or a zero by manipulation of the control word odd/even parity select bit (BD12) for each word transmitted.

The receivers automatically count the number of "ones" in the incoming ARINC word (including the parity bit) and then changes the 32nd bit to reflect odd parity. The user can calculate the value of the original 32nd bit received.

The above methods require additional software overhead, but allow the user to utilize industry standard ARINC 429 hardware to meet the ARINC 575 specification.

Question #8

Why don't ARINC transmitters have more output drive capability?

Answer:

This is the result of a requirement of the ARINC specification. The transmitter output impedance is required to have a nominal value of 75 ohms. This results in lowering the drive capability of the ARINC transmitters, especially when driving cables that do not have a 75 ohm characteristic impedance.

Question #9:

May I operate the HI-8382 with $\pm$12V supplies?

Answer:

Yes. The device will work fine with the lower supply voltages.

Question #10:

Must the CLOCK input on the HI-8382 be tied to the TX CLK output of the HI-8282?

Answer:

No. The CLOCK input is tied to the +5V supply for ARINC 429 applications.

General Notes

The majority of all applications problems encountered with the HI-8282 involve the control word register. Many of the problems result from the control word register not receiving the control word data due to incorrect chip addressing.

Anytime an application problem arises, it is always best to begin troubleshooting by attaching scope probes to the parallel data bus and the $\overline{CWSTR}$ input and then writing the control word. This will ensure that the correct data is getting to the control word register.

Applications Support

The answers to the questions posed above are intended as guidelines for troubleshooting; however, there could be any number of reasons for why a particular problem is occurring. Users are encouraged to call Holt's applications support staff when an applications problem is encountered.